
**DisplayPort™ Standard**

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# DisplayPort Standard

**Version 1**

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## Purpose

The purpose of this document is to define a flexible digital interface capable of handling video and audio data over a common cable.

## Summary

DisplayPort™ specifies an open digital communications interface for use in common within both internal connections, such as interfaces within a PC or monitor, and external display connections, including interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display.

## *Preface*

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| Holder Name | Contact Information | Claims Known |
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| Genesis Microchip Inc. | Jeffrey Lin<br>(jeffrey.lin@gnss.com) | Pending U.S. Patent Applications<br>10/726,794 (Claims 1-3, 5-23, 26-44, 45, and 46)<br>10/726,802 (Claims 2-7, 9-14, and 16-20)<br>10/726,438 (Claims 2-22, and 24-27)<br>10/727,131 (Claims 1-16)<br>10/726,440 (Claims 1-33)<br>10/726,350 (Claims 2-18)<br>10/726,362 (Claims 1-18)<br>10/726,895 (Claims 1-18)<br>10/726,441 (Claims 1-3, and 5-17)<br>10/726,934 (Claims 1-8) |
| JAE Electronics, Inc. | Mark Saubert<br>(saubertm@jae.com) | U.S. Patent<br>6,315,616 (Claims 9, 11, 14)<br><br>Pending U.S. Patent Application<br>10/287,925 |
| Molex Inc. | Scott Sommers<br>(scott.Sommers@molex.com) | U.S. Patent<br>6,280,209 (at least Claim 1)<br>6.457,983 (at least Claims 1 and 23)<br>6,575,789 (at least Claim 1)<br><br>Pending U.S. Patent Applications<br>10/246,289<br>11/190,138 |

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## *Acknowledgements*

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# 1 Introduction

DisplayPort is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and CE industries. It consolidates internal and external connection methods to reduce device complexity, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

## *1.1 DisplayPort Specification Organization*

The DisplayPort specification is organized into the following sections that define the overall architecture and structure of the display interface:

Chapter 1 –Introduction

The Introduction chapter defines the high level industry needs for DisplayPort, and the resulting technical objectives that the protocol, electrical, and mechanical sections are intended to satisfy. This chapter also includes a glossary of terms for the overall specification, references, and overview of DisplayPort architecture.

Chapter 2 – Link Layer

The Link Layer chapter describes the protocol specification for configuring and managing the flow of data over both the forward transport channel and the auxiliary bi-directional channel.

Chapter 3 – Physical Layer

The Physical Layer chapter describes the electrical specification for defining DisplayPort transmitter and receiver implementations. The physical layer specification defines the required circuitry and encoding methodology for electrically transmitting data to and from the DisplayPort link layer over a cable or circuit board traces.

Chapter 4 – Mechanical

The Mechanical chapter describes the connector and cable specification for defining internal and external DisplayPort connectors used to convey the electrical signals defined by the DisplayPort physical layer.

Chapter 5 – Source/Sink Device Interoperability

The Device and Link Media Requirements chapter describes the device and display format requirements to support interoperability between Source and Sink Devices that implement DisplayPort connections.

## *1.2 DisplayPort Objectives*

This DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability for broad application within PC and CE devices. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. Potential internal chip-to-chip applications include usage within a notebook PC for driving a panel from a graphics controller, and usage within a monitor or TV for driving the display component from a display controller. Examples of box-to-box applications for DisplayPort include display connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

DisplayPort is architected to meet several key needs within the PC and CE industry as defined in Section 1.2.1. These industry needs are further translated here into a set of technical objectives in Section 1.2.2 for the DisplayPort specification to ensure that the display interface can support current and future industry requirements. Specific objectives for both external and internal display connections are also

further defined in sections 1.2.3 and 1.2.4 for the DisplayPort specification. Section 1.2.5 defines the additional objectives for application to CE devices.

### 1.2.1 Key Industry Needs for DisplayPort

The following PC and CE industry needs were considered in the development of the DisplayPort architecture and resulting interface specification:

1) Drive maximum application and re-use of digital technology to enable reduced device costs associated with implementing a digital display connection.
2) Enable a common signaling methodology for both internal and external display connections to reduce device complexity and promote commoditization.
3) Enable an extensible architecture that supports an optional robust content protection capability that may be economically implemented.
4) Enable high quality optional digital audio transmission capability.
5) Enable higher levels of silicon integration and innovation within rendering and display devices to reduce device complexity and enable digital interface commoditization. Examples of potential DisplayPort integration capability include transmitter integration within a graphics or display controller, and receiver integration within a timing controller on a panel.
6) Simplify cabling for internal and external digital display connections.
7) Address performance concerns with existing technologies by providing higher bandwidth over fewer wires.
8) Apply embedded clock architecture to reduce EMI susceptibility and physical wire count.
9) Provide a small form factor connector that can be plugged in by feel, and whose design will enable four connectors to be placed on a full height PCI card bracket.
10) Ensure broad PC and CE industry deploy-ability via an open and extensible industry standard

DisplayPort addresses these industry needs by defining an electrical and protocol specification that may be readily implemented in panel timing controllers, graphics processors, media processors, and display controllers.

A forward drive channel is defined that is scalable from 1-4 lanes, and implements a micro-packet architecture that can support variable color depths, refresh rates, and display resolutions. A bi-directional return channel is defined that also implements micro-packet architecture for flexible delivery of control and status information.

DisplayPort includes a mechanical specification that defines a small, user-friendly external connector that is optimized for use on thin profile notebooks in addition to allowing up to four connectors on a graphics card. A standard panel connector for internal applications is also defined within the mechanical section of the specification.

### 1.2.2 DisplayPort Technical Objectives

The cross industry needs defined for DisplayPort above may be defined further through translation into specific technical objectives. These technical objectives for DisplayPort are:

1) Provides a high bandwidth forward transmission link channel, with a bi-directional auxiliary channel capability.

2) Provides application support for up to 10 Gbps forward link channel throughput to address long term PC industry needs to support greater than QXGA (2048 x 1536) resolution and greater than 24 bit color depths.

3) Provides application support for up to 1 Mbps auxiliary channel throughput with a maximum latency of 200 micro-seconds

4) Supports variable color depth transmission (6, 8, 10, 12, 16 bits per component)

5) Supports EMI compliance to FCC B standard with 6db of margin

6) Supports existing VESA and CEA standards where applicable.

7) Architecture does not preclude legacy transmission support (e.g. DVI and LVDS) to and from DisplayPort components.

8) Supports Hot Plug and Unplug detection and link status-failure detection

9) Supports full bandwidth transmission via direct drive over a 3 meter cable.

10) Supports reduced bandwidth transmission via direct drive over a 15 meter cable. DisplayPort supports a minimum of 1080p resolution at 24bpp, 50/60 Hz over 4 lanes at 15 meters.

11) Supports audio skew of less than 1ms

12) Supports a bit error rate of $10^{-9}$ for raw transport per lane, and $10^{-12}$ symbol error rate for audio and control data after ECC encoding / decoding.

13) Supports sub 65 nanometer (0.065 micron) process technologies for integration in Source Devices, and supports 0.35 micron process technologies for integration in Sink Devices.

### 1.2.3 DisplayPort External Connection Objectives

For external connections between Source Device and Sink Device, the DisplayPort specification is designed to address the following technical objectives:

1) Supports reading of the display EDID whenever the display is connected to power, even an AC-trickle power.

2) Supports DDC/CI and MCCS command transmission when the monitor includes a display controller.

3) Supports external display configurations that do not include scaling, a discrete display controller, or on screen display (OSD) functions, enabling low cost, digital monitors.

4) For external notebook PC applications, DisplayPort allows potential support for direct drive through a docking connector configuration. A repeater function in the dock is strongly recommended.

5) The external DisplayPort connector is identical for all display applications and provides support for 4 lanes. Captive cables may support 1, 2, or 4 lanes to reduce cost.

6) The external DisplayPort connector includes a multi-purpose power pin.

7) The external DisplayPort connector is symmetrical such that the same connector may be used on both Source and Sink Devices.

8) The external DisplayPort connector supports a blind connection by feel without the need for visual alignment.

9) The external DisplayPort connector is sized to allow 4 connectors to fit on a standard full height ATX/BTX bracket opening for PCI, AGP, and PCI-Express add in cards.

### 1.2.4 DisplayPort Internal Connection Objectives

For internal connections such as within a notebook PC, or within a monitor, the DisplayPort specification is designed to address the following technical objectives:

1) DisplayPort defines a common panel connector to simplify internal device connections.
2) The number of lanes in the internal cable is implementation dependent, and may be 1, 2, or 4.
3) Internal DisplayPort connections may support both maximum and reduced link bandwidths.
4) Internal DisplayPort connections support low link power modes.
5) Hot Plug support for internal DisplayPort connections is implementation dependent.

### 1.2.5 DisplayPort CE Connection Objectives

For application to consumer electronics devices, the DisplayPort specification is designed to address the following technical objectives:

1) DisplayPort optionally delivers digital audio concurrent with display data.
2) Provides support for maintaining synchronization for delivery of audio and video data to within +/- 1ms.
3) DisplayPort architecture supports an optional robust content protection capability that may be economically implemented.
4) DisplayPort supports equivalent functionality to the feature sets defined in CEA-861-C for transmission of high quality uncompressed audio-video content, and CEA-931-B for the transport of remote control commands between Sink and Source Devices.
5) DisplayPort supports variable audio formats, audio codings, sample frequencies, sample sizes, and audio channel configurations. DisplayPort supports up to 8 channels of LPCM coded audio at 192 kHz with a 24 bit sample size.
6) DisplayPort supports variable video formats based on flexible aspect, resolution, and refresh combinations based on the VESA DMT and CVT timing standards and those listed in CEA-861-C standard.
7) DisplayPort supports industry standard colorimetry specifications for consumer electronics devices including RGB and YCbCr. 4:2:2 and YCbCr 4:4:4.

### 1.2.6 Content Protection for DisplayPort

For implementations of the DisplayPort interface where content protection is desired, it is recommended that DPCP (Display Port Content Protection) Version 1.0 be used. This is recommended in order to minimize incompatibilities between DP devices in the market.

## 1.3 Acronyms

| Acronym | Stands For: |
|---|---|
| API | Application Programming Interface. |
| BER | Bit Error Rate |
| bpc | Bits Per Component |
| bpp | Bits Per Pixel |
| CDR | Clock-to-Data Recovery |
| CEA | Consumer Electronics Association |
| CP | Content Protection |
| CVT | Coordinated Video Timings |
| DB | Data Byte |
| DDC/CI | Display Data Channel/Command Interface |
| DPCP | DisplayPort Content Protection |
| DPCD | DisplayPort Configuration Data |
| DJ | Deterministic Jitter |
| DMT | Discrete Monitor Timing |
| DP | DisplayPort |
| ECC | Error Correcting Code |
| E-DDC | Enhanced Display Data Channel |
| EDID | Extended Display Identification Data |
| EOS | Electrical Over-Stress |
| ESD | Electro Static Discharge |
| GPU | Graphics Processor Unit |
| HB | Header Byte |
| HPD | Hot Plug Detect |
| LFSR | Linear Feedback Shift Register. |
| LSB | Least Significant Bit |
| Maud | M value for audio |
| MCCS | Monitor Control Command Set |
| MSB | Most Significant Bit |
| Mvid | M value for video |
| Naud | N value for audio |
| nb | nibble |
| Nvid | N value for video |
| NORP | Number Of Receiver Ports |
| PB | Parity Byte |
| PCB | Print Circuit Board |
| PRBS | Pseudo Random Bit Sequence |
| RJ | Random Jitter |
| RTL | Register Transfer Level |
| TCON | Timing CONtroller |
| TDR | Time Domain Reflectometry |
| TIA | Timing Interval Analyzer |
| TU | Transfer Unit |
| UI | Unit Interval |
| VB-ID | Vertical Blanking ID |
| VESA | Video Electronics Standard Association |

| | |
|---|---|
| VHDL | Very high speed integrated circuit Hardware Description Language |

## 1.4 Glossary

| Terminology | Definition |
|---|---|
| ANSI 8B/10B | Channel coding specification as specified in ANSI X3.230-1994, clause 11 |
| AUX CH | Half-duplex, bi-directional channel between DisplayPort transmitter and DisplayPort receiver. Consists of 1 differential pair transporting self-clocked data. The DisplayPort AUX CH supports a bandwidth of 1Mbps over DisplayPort link. DisplayPort Source Device is the master (also referred to as AUX CH Requester) that initiates an AUX CH transaction. DisplayPort Sink Device is the slave (also referred to as AUX CH Replier) that replies to the AUX CH transaction initiated by the Requester. |
| Box-to-box connection | DisplayPort link between two boxes detachable by an end user. A DisplayPort cable-connector assembly for the box-to-box connection shall have four Main Link lanes. |
| bpc | Number of bits for each of R,G, B or Y, Cb, and Cr. |
| bpp | Number of bits for each pixel. For RGB and YCbCr444, the bpp value is 3x the bpc value. For YCbCr422, the bpp value is 2x the bpc value. |
| Captive cable | DisplayPort cable that is attached to Sink Device and cannot be detached by an end user. Captive DisplayPort cable may have one, two, or four Main Link lanes, while end-user-detachable cable is required to have four Main Link lanes. |
| Branch Device | Devices located in between Root (Source Device) and Leaf (Sink Device). Those devices are:<br>- Repeater Device,<br>- DisplayPort-to-Legacy Converter,<br>- Legacy-to-DisplayPort Converter,<br>- Replicater Device,<br>- Composite Device.<br><br>For definitions of these Branch Devices, refer to Section 2.1.4 on p.29. |
| CEA range | Nominal zero intensity level at 16 for 24-bpp, 64 for 30-bpp, 256 for 36-bpp, and 1024 for 48-bpp. Maximum intensity level at maximum code value allowed for bit depth, namely, 235 for 24-bpp RGB, 940 for 30-bpp RGB, 3760 for 36-bpp RGB, and 15040 for 48-bpp RGB. Note that the RGB CEA range is defined for 24, 30, 36, 48 bpp RGB only, not for 18-bpp RGB. |
| Debouncing Timer | A timer that counts the "debouncing period" to elapse after a mechanical contact (for example, plugging in a cable-connector assembly to a receptacle connector) to give the signals on the connectors to settle. |
| De-spreading | An operation by Sink Device for getting rid of down-spread of the stream clock when the clock is regenerated from the down-spread link symbol clock. |
| DisplayPort Content Protection (DPCP) | Content protection system for the DisplayPort link. DPCP is a separate specification from the DisplayPort specification. |
| DisplayPort receiver | Circuitry that receives the incoming DisplayPort Main Link data. Also contains the transceiver circuit for AUX CH. Located in a device with DisplayPort Sink Function. |
| DisplayPort transmitter | Circuitry that transmits the DisplayPort Main Link data. Also contains the transceiver circuit for AUX CH. Located in a device with DisplayPort Source Function. |
| DisplayPort Configuration Data (DPCD) | Mapped to the DisplayPort address space of DisplayPort Sink Device. DisplayPort Source Device reads the receiver capability and status of the DisplayPort link and the Sink Device from DPCD address. Furthermore, |

| | |
|---|---|
| | DisplayPort Source Device writes to the link configuration field of DPCD for configuring and initializing the link. |
| Down-spread | Spreading a clock frequency downward from a peak frequency. As compared to “center-spread”, avoids exceeding the peak frequency specification. |
| Embedded connection | DisplayPort link within a box that is not to be detached by an end user. DisplayPort cable for the embedded connection may have one, two, or four Main Link lanes. |
| Gen-lock | Locking the output timing of a circuit to the input timing. For example, the DisplayPort receiver may Gen-lock its DE output timing to the timing of DE signal it receives from a transmitter on the other end of the link. |
| HPD Pulse | There are two kinds of HPD pulse depending on the duration.<br>- Sink Device, when issuing an IRQ (interrupt request) to Source Device, shall generate a low-going HPD pulse of 0.5ms - 1ms in duration. Upon detecting this “IRQ HPD pulse”, Source Device shall read link/sink status field of DPCD and take corrective action.<br>- When Source detects a low-going HPD pulse longer than 2ms in duration, it shall be regarded as Hot-plug-event HPD pulse. Upon detecting this Hot-plug-event HPD pulse, Source shall read receiver capability field and link/sink status field of DPCD and take corrective action. |
| Idle Pattern | Link symbol pattern sent over the link when the link is active with no stream data being transmitted. |
| Leaf Device | Sink Device, located at a leaf in a DisplayPort tree topology. |
| Link Clock Recovery | Operation of recovering the link clock from the link data stream. |
| Link Layer | Server providing services as instructed/requested by the Stream-/Link-Policy Makers. |
| Link Policy Maker | Manages the link and is responsible for keeping the link synchronized. All DisplayPort Devices shall have Link Policy Maker. |
| Link Symbol Clock | Link Symbol Clock frequency is 270MHz for 2.7Gbps per lane, while it is 162MHz for 1.62Gbps per lane. |
| Main Link | Uni-directional channel for isochronous stream transport from DisplayPort Source Device to DisplayPort Sink Device. Consists of 1, 2, or 4 lanes, or differential pairs. Supports 2 bit rates: 2.7Gbps per lane (referred to as “high bit rate”) and 1.62Gbps per lane (referred to as “low bit rate” or “reduced bit rate”). |
| Main Stream Attributes | Attributes describing the main video stream format in terms of geometry and color format. Inserted once per video frame during the video blanking period. Used by DisplayPort receiver for reconstructing the stream. |
| Physical Layer (PHY) | Consists of Logical and Electrical Sub-blocks. Physical Layer decouples data transmission electrical specifications from the DisplayPort Link Layer. |
| PRBS7 | 7-bit pseudo random bit sequence. |
| Rendering Function | Function of displaying/portraying/storing/processing stream data. For example, video display, speaker, optical recorder, and hard disk drive recorder. |
| Root Device | Source Device, located at a root in a DisplayPort tree topology. |
| Secondary Data | Data transported over Main Link that are not main video stream data. Audio data and InfoFrame packet are examples. |
| Sink Device | Contains one Sink Function and at least one Rendering Function, and is a Leaf Device in a DisplayPort tree topology. |
| Sink Function | Sink functionality (reception of stream) of DisplayPort |
| Source Device | Contains one or more Source Functions and is a root in a DisplayPort tree topology. |
| Source Function | Source functionality (transmission of stream) of DisplayPort |

| | |
|---|---|
| Stream Clock | Used for transferring stream data into DisplayPort transmitter within DisplayPort Source Device or from DisplayPort receiver within DisplayPort Sink Device. Video and audio (optional) are likely to have separate stream clocks |
| Stream Clock Recovery | Operation of recovering the stream clock from the Link Symbol Clock. |
| Stream Policy Maker | Manages how to transport an isochronous stream. |
| Symbol | There are Data Symbols and Control Symbols. Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as "ANSI 8B/10B" in this document) before being transmitted over a link. In addition to data symbols, DisplayPort Ver.1.0 defines nine Control Symbols for framing Data Symbols. Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes). |
| TCON | Timing Controller circuit that output control and data signals to driver electronics of a display device. |
| Time Stamp | A value used by a clock circuit in order to keep two systems synchronized |
| Transfer Unit (TU) | Used to carry main video stream data during its horizontal active period. TU has 64 symbols per lane (except for at the end of the horizontal active period), each consisting of active data symbols and fill symbols. |
| Trickle Power | Power for Sink Device that is sufficient to let Source Device read EDID via AUX CH, but insufficient to enable Main Link and other Sink functions. For Sink to drive Hot Plug Detect (HPD) signal high, at least the trickle power must be present. The amount of power needed for the trickle power is Sink implementation specific. |
| VB-ID | Data symbol indicating whether the video stream is in vertical blanking interval, whether video stream is transported, and whether to mute audio. |
| VESA range | Nominal zero intensity level at code value zero. Maximum intensity level at maximum code value allowed for bit depth, Namely, 63 for 18-bpp RGB, 255 for 24-bpp RGB, 1023 for 30-bpp RGB, 4095 for 36-bpp RGB, and 65,535 for 48-bpp RGB. |
| Via | A cross-over between layers of multi-layer PCB (print circuit board) |
| Video Horizontal Timing | Horizontal timing means video line timing. For example, horizontal period and horizontal sync pulse mean line period and line sync pulse, respectively.<br>Vertical timing means video frame (or field) timing. For example, vertical period and vertical sync pulse mean a frame (or field) period and a frame sync pulse, respectively.<br>The terms, "horizontal" and "vertical", do not necessarily correspond to the physical orientation of a display device. For instance, a line may be oriented vertically on a "portrait" display. |
| Video Vertical Timing | |

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## *1.6 Overview of DisplayPort*

DisplayPort link consists of Main Link, Auxiliary Channel (AUX CH), and Hot Plug Detect (HPD) signal line.

As shown Figure 1.1 below, Main Link is a uni-directional, high-bandwidth, and low-latency channel used for transport of isochronous streams such as uncompressed video and audio. Auxiliary Channel is a half-duplex bidirectional channel used for link management and device control. HPD signal also serves as an interrupt request by Sink Device.

In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter.

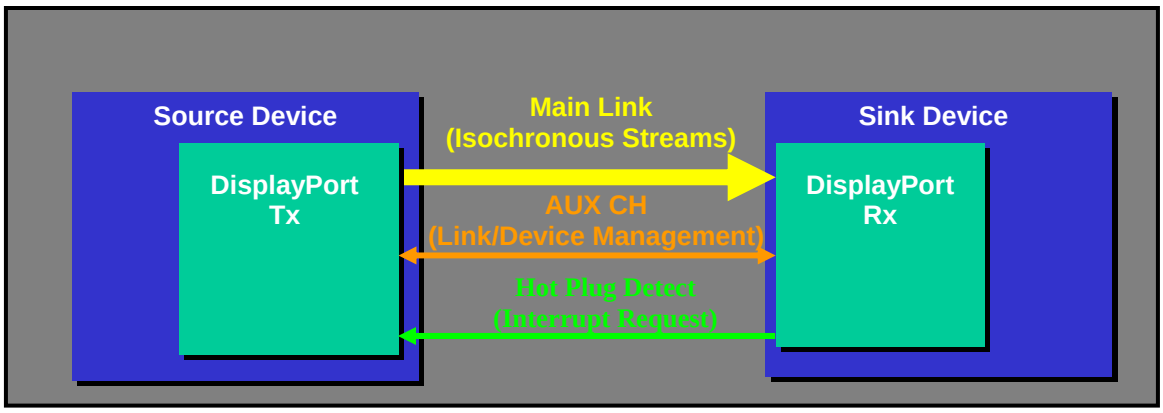



**Figure 1.1 Make-up of DisplayPort Data Transport Channels**

### 1.6.1 Make-up of Main Link

Main Link consists of AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages.

Two link rates are supported: 2.7Gbps and 1.62Gbps per lane. The link rate is decoupled from the pixel rate. The pixel rate is regenerated from the link symbol clock using the time stamp values M and N. The capabilities of the DisplayPort transmitter and receiver, and the quality of the channel (or a cable) will determine whether the link rate is set to 2.7Gbps or 1.62Gbps per lane.

The number of lanes of Main Link is 1, 2, or 4 lanes. The number of lanes is decoupled from the pixel bit depth (bits per pixel, or bpp) and component bit depth (bits per component, or bpc). Component bit depths of 6, 8, 10, 12, and 16 are supported with the colorimetry formats of RGB, YCbCr444/422 in DisplayPort Ver.1.0 regardless of the number of Main Link lanes.

All the lanes carry data: There is no dedicated clock channel. The clock is extracted from the data stream itself that is encoded with ANSI 8B/10B coding rule (the channel coding specified in ANSI X3.230-1994, clause 11).

Source and Sink Devices are allowed to support the minimum number of lanes required for their needs. The devices that support 2 lanes are required to support both 1 and 2 lanes, while those that support 4 lanes are required to support 1, 2, and 4 lanes. The external cable that is detachable by an end user is required to support 4 lanes for maximizing the interoperability between Source Device and Sink Device.

Excluding the 20% channel coding overhead, DisplayPort Main Link provides for the application bandwidth (also called link symbol rate) as shown below:

- Link rate = 2.7Gbps
  - 1 lane = 270Mbytes per second
  - 2 lanes = 540Mbytes per second
  - 4 lanes = 1080Mbytes per second
- Link rate = 1.62Gbps
  - 1 lane = 162Mbytes per second
  - 2 lanes = 324 Mbytes per second
  - 4 lanes = 648Mbytes per second

DisplayPort devices may freely trade pixel bit depths with resolution and frame rate of a stream within the available bandwidth. Examples are shown below.

- Over 4 lanes
  - 12-bpc YCbCr444 (36 bpp), 1920x1080p @ 96Hz
  - 12-bpc YCbCr422 (24 bpp), 1920x1080p @ 120Hz
  - 10-bpc RGB (30 bpp), 2560x1536 @ 60Hz
- Over 1 lane
  - 10-bpc YCbCr444 (30 bpp), 1920x1080i @60Hz
  - 6-bpc RGB (18 bpp), 1680x1050 @60Hz

The data mapping of a stream to Main Link is devised to facilitate the support of various lane counts. For example, the pixel data is packed and mapped over 4-lane Main Link as follows, regardless of the pixel bit depth and colorimetry format:

- Pixel data mapping over 4-lane Main Link
  - Pixels 0, 4… : Lane 0,
  - Pixels 1, 5… : Lane 1
  - Pixels 2, 6… : Lane 2
  - Pixels 3, 7… : Lane 3

The stream data is packed into "Micro-Packet" which is called "Transfer Unit". The Transfer Unit is 64 link symbols long per lane. After the stream data is packed and mapped to Main Link, the packed stream data rate will be equal to or smaller than the link symbol rate of Main Link. When it is smaller, stuffing symbols are inserted.

During the horizontal and vertical blanking period of the main video stream, almost all the link symbols are stuffing symbols, which may be substituted with stream attribute packet (containing the image height, width, etc. of the main video stream) used for regenerating the stream in Sink Device, and optional secondary-data packets such as audio stream packets.

### 1.6.2 Make-up of AUX CH

AUX CH consists of an AC-coupled, doubly terminated differential pair. Manchester II coding is used as the channel coding for AUX CH. As is the case with Main Link, clock is extracted from the data stream.

AUX CH is half-duplex, bi-directional. Source Device is the master and Sink Device the slave. Sink Device may toggle the HPD signal to interrupt Source Device which would prompt an AUX CH request transaction.

AUX CH provides for 1Mbps of data rate over the supported cable lengths of up to 15m and longer. Furthermore, each transaction takes no more than 500 us (the maximum burst data size = 16 bytes), thus avoids one AUX CH application from starving other applications.

### 1.6.3 Link Configuration and Management

Upon Hot Plug Detection, Source Device configures the link through Link Training. A proper number of lanes get enabled at a proper link rate with a proper drive current/equalization level, through the handshake between DisplayPort transmitter and receiver via AUX CH.

During normal operation following Link Training, Sink Device may notify the link status change, for example, loss of synchronization, by toggling HPD signal, thus sending an interrupt request. Source Device, then checks the link status via AUX CH and takes corrective action. This closed-loop link operation enhances the robustness and interoperability between Source Device and Sink Device.

Since the link rate is decoupled from the stream rate, DisplayPort link may stay active and stable even when the timing of a transported stream changes.

### 1.6.4 Layered, Modular Architecture

Figure 1.2 shows the layered architecture of DisplayPort.

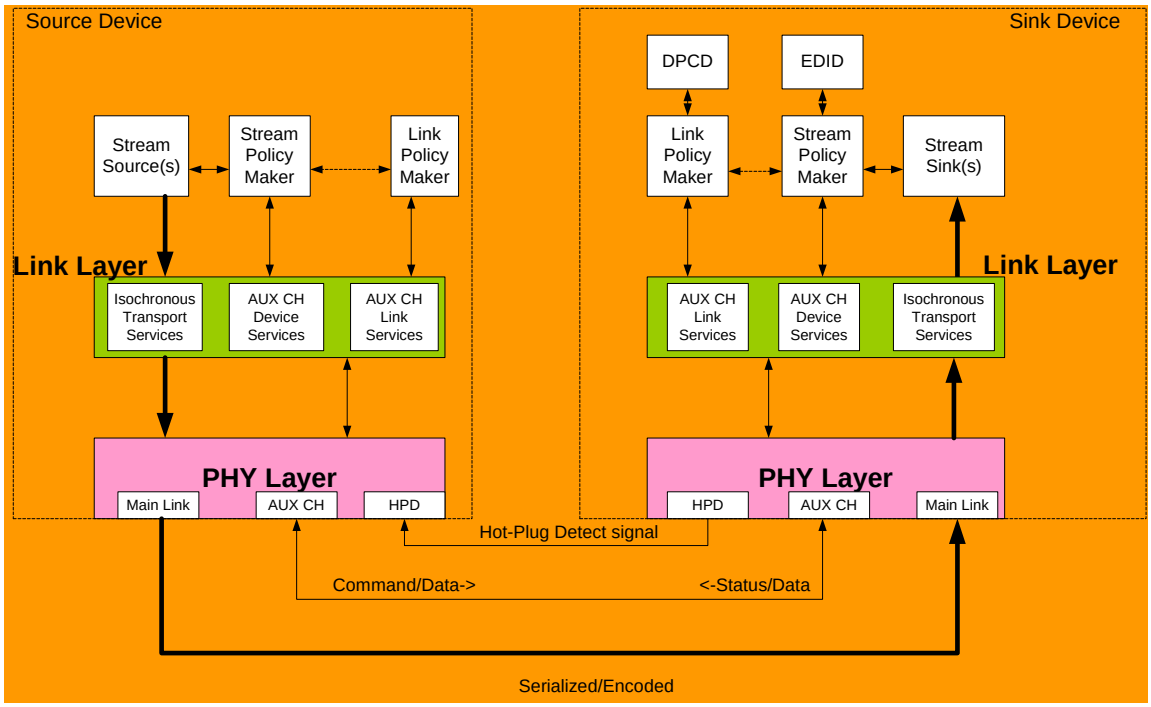



**Figure 1.2 Layered Architecture**

In Figure 1.2 above, DPCD (DisplayPort Configuration Data) in Sink Device describes the capability of the receiver, just as EDID describes that of the Sink Device. Link and Stream Policy Makers manages the

link and the stream, respectively. How they are implemented (state machine, firmware, or system software) is implementation specific.

It should be noted that Physical Layer may be replaced in the future while the Link Layer stays intact. As the technology that is the most effective in terms of cost and performance evolves over time, DisplayPort specification will be able to evolve.

Furthermore, micro-packet-based transport enables a seamless extension of the DisplayPort specification toward supporting multiple audio-visual streams and other data types. Switches and hubs may be used to micro-packet-switch streams among multiple Source Device and Sink Device.

As for content protection, it is recommended that DPCP (DisplayPort Content Protection) Ver.1.0 be used for those DisplayPort implementations where contention protection is desired.

# 2 Link Layer

## 2.1 Introduction

This chapter describes the services provided by the Link Layer of DisplayPort. These services are:

- Isochronous transport services over Main Link

  The isochronous transport services map the video and audio streams into Main Link with a set of rules (as explained in Section 2.2.1 on p.33), so that the streams can be properly re-constructed into the original format and time base in the Sink Device.

- Link and device management services over AUX CH

  Link services are used for discovering, configuring, and maintaining the link (as explained in Section 2.5.3 on p.96). The AUX CH read/write access to DPCD (DisplayPort Configuration Data) address is used for these purposes. The device services support device-level applications such as EDID read and MCCS control (Section 2.5.4 on 110). Furthermore, AUX CH may be used for optional content protection.

In conjunction with the description of these services, AUX CH states/arbitration/ transaction syntax are also covered in this chapter.

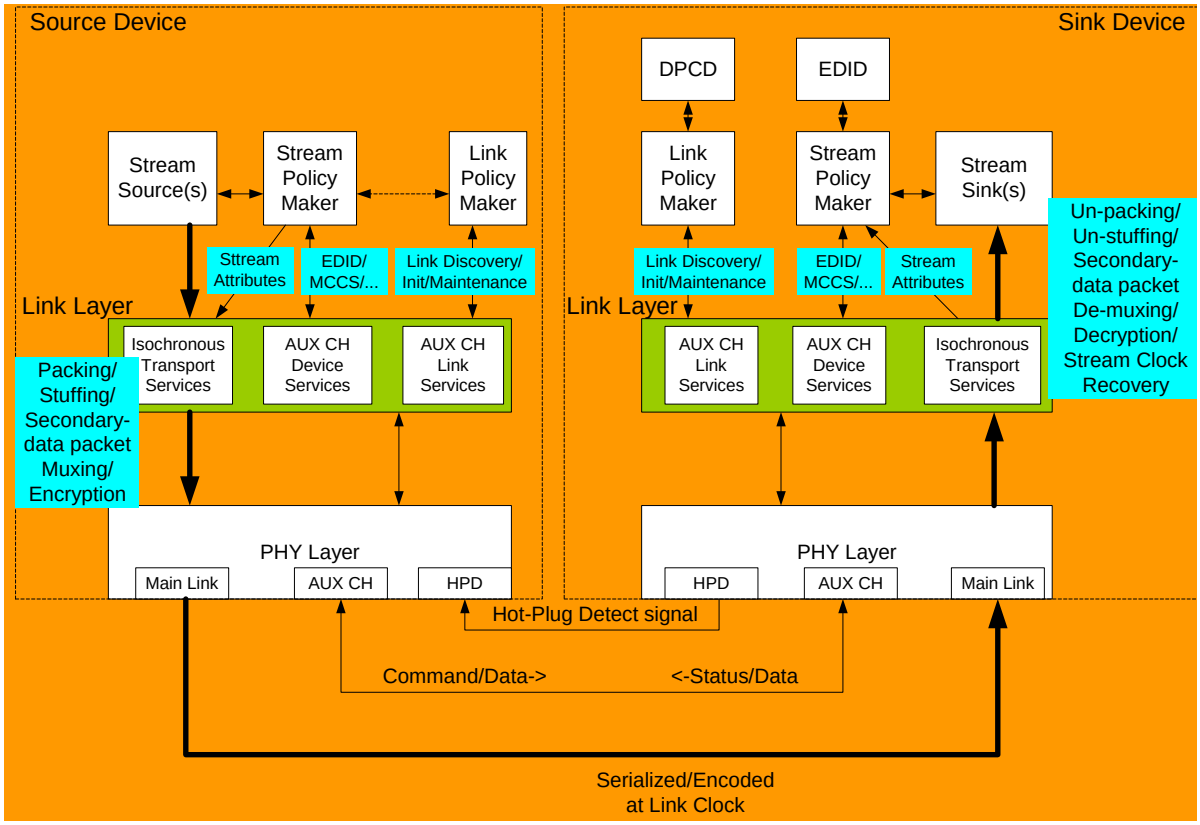



**Figure 2.1 Overview of Link Layer Services**

The Link Layer provides services as instructed/requested by the Stream-/Link-Policy Makers (Figure 2.1). Stream Policy Maker manages how to transport the stream. Link Policy Maker manages the link and is responsible for keeping the link synchronized. In this chapter (and in the entire DisplayPort

specification as well), only the semantics of the interactions between Policy Makers and Link Layer are described. The syntax of these interactions (that is, API) is implementation-specific, and is beyond the scope of this document.

### 2.1.1 Number of Lanes and Per-lane Data Rate

The DisplayPort Specification Ver.1.0 supports three options for the number of Main Link lanes and two options for Main Link data rate per lane as follows:

- 4, 2, or 1 lanes
- 2.7 or 1.62 Gbps per lane

The Link Layer specification (data mapping specification, in particular) is defined to facilitate the support of these lane-count options.

The per-lane data rate shall be determined not only by the capabilities of DisplayPort transmitter/receiver but also by the quality of a channel, or a cable. The DisplayPort Sink Device shall indicate the capability of its receiver in the Receiver Capability field of DPCD, as described in Section 2.5.3.1 on p.97. Upon reading the Receiver Capability, the DisplayPort Source Device shall configure the link by writing to the Link Configuration field of DPCD in DisplayPort Sink Device and running Link Training. Through this process of receiver capability discovery and link training, DisplayPort Source Device and DisplayPort Sink Device shall be able to negotiate for the optimal lane-count and per-lane data rate for a given connection.

### 2.1.2 Number of Main, Uncompressed Video Streams

The scope of DisplayPort Specification Ver.1.0 is limited to a transport of a single, uncompressed video stream as the Main Stream, with optional insertion of secondary-data packet such as audio stream packet. Transport of multiple Main Streams is not covered in Ver.1.0. However, the DisplayPort Specification is constructed in a way that can be seamlessly extended for supporting transport of multiple uncompressed video streams and other data types.

### 2.1.3 Basic Functions

The basic functions of DisplayPort Devices are described below.

- Source Function – the source functionality (that is, transmission of stream) of DisplayPort
- Sink Function – the sink functionality (that is, reception of stream) of DisplayPort

Rendering Function - Displays/portrays/stores/image-processes the received stream: Examples are video display, speaker, optical recorder, hard disc drive recorder, etc.

### 2.1.4 DisplayPort Device Types and Link Topology

A device will contain at least one DisplayPort function as well as other functions such as a display, speakers, recording device or even an entire computer.

DisplayPort Specification Ver.1.0 shall cover the following device types:

- Source Device - a device that contains one or more Source Functions and is a root in a DisplayPort tree topology.
- Sink Device – a device that contains a single Sink Function and at least one Rendering Function and is a leaf in a DisplayPort tree topology.

- Repeater Device (1 in, 1 out) – a device that contains one Sink Function and one Source Function.
- Legacy-to-DisplayPort Converter (1 in, 1 out) – a device that contains a one Legacy Sink Function and one DisplayPort Source Function.
- DisplayPort-to-Legacy Converter (1 in, 1 out) – a device that contains one DisplayPort Sink Function and one Legacy Source Function.
- Replicater Device (1 Sink Function, k Source Functions, where k is a positive integer > 1). This device may include a Legacy Converter Sink and/or one or more Legacy Converter Sources. Each Legacy Converter Source will be deemed a Rendering Function by the DPCP system.
- Concentrator Device (k Sink Functions, 1 Source Function, where k is a positive integer >1)
- Composite Device – a Replicater with a Rendering Function, For example, a display monitor that has one or more downstream ports. Format converter that alters the stream (for example, format conversion) is regarded as Composite Device. If one of the outputs on a Replicater is a Legacy Converter then that output will be deemed a Rendering Function.

DisplayPort Device with Source Function and/or Sink Function shall have Link Policy Maker. Source Device that originates or processes (for example, format conversion) the stream data and Sink Device shall have Stream Policy Maker as well.

DisplayPort Device with Sink Function shall have DPCD. Sink Device and Composite Device shall have EDID as well

Using the above device types, DisplayPort networks consisting either of a single hop or multiple hops (daisy chain or tree) may be configured.

From the perspective of the device location within a link, the devices are categorized as follows:

- Root Device = Source Device
- Leaf Device = Sink Device
- Branch Device = Devices other than Source Device and Sink Device described above.

In DisplayPort Specification Ver.1.0, DisplayPort Source Device shall be link-topology agnostic: Source Device shall not inquire, for example, how many downstream ports its immediate downstream device has or how many downstream hops are present in its downstream link. Source Device needs only to read the Sink Device capability (EDID) and the link capability (DPCD) from its immediate downstream device and to source a stream accordingly.

For DisplayPort Content Protection (DPCP), Source Device shall find out how many devices containing Rendering Function are connected to the network of devices and take action if there are too many such functions. The DisplayPort Specification is defined in a way that such CP discovery can be accomplished without any Function or Device having knowledge of network topology.

Figure 2.2 - Figure 2.7 show some of the examples of DisplayPort link topologies.

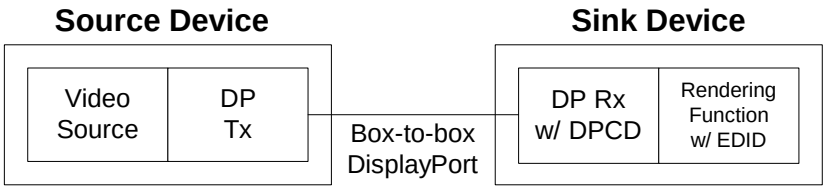



**Figure 2.2 Single-hop, Detachable DisplayPort Link**

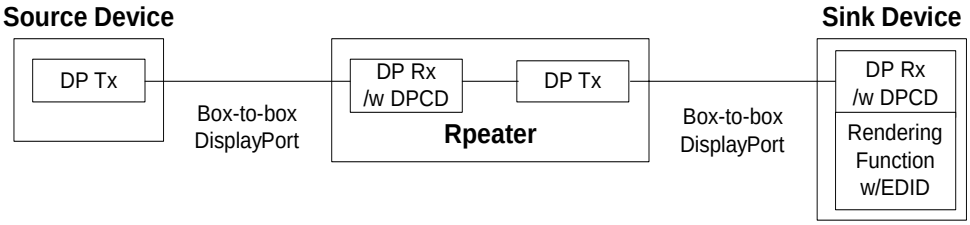



**Figure 2.3 DisplayPort Source Device to DisplayPort Sink Device via Repeater**

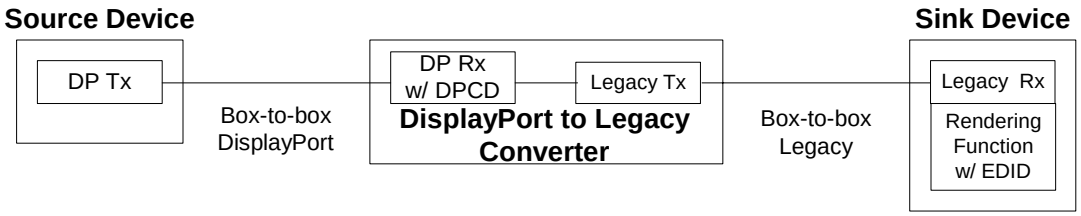



**Figure 2.4 DisplayPort Source Device to Legacy Sink via DisplayPort-to-Legacy Converter**

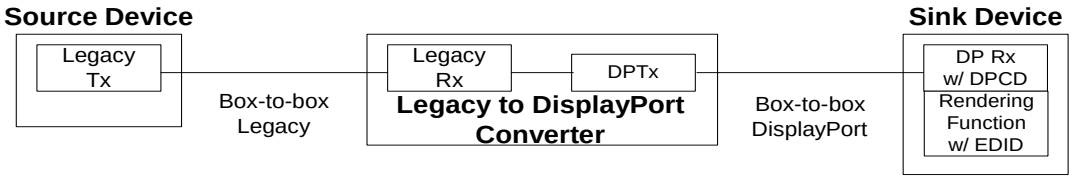



**Figure 2.5 Legacy Source Device to DisplayPort Sink Device via Legacy-to-DisplayPort Converter**

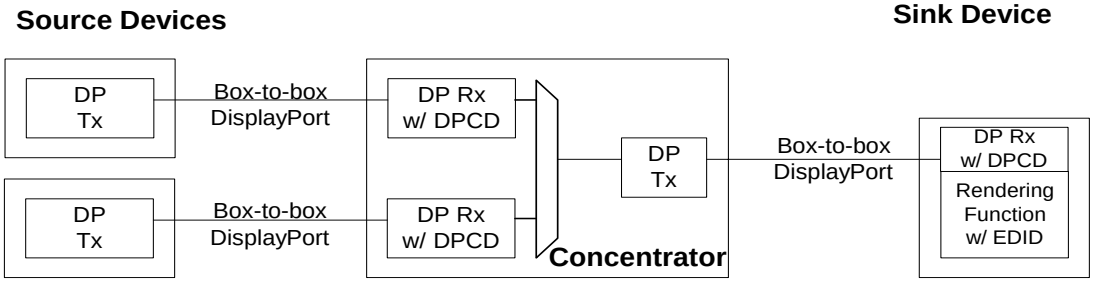



**Figure 2.6 Multiple Source Devices to Sink Device via Concentrator**

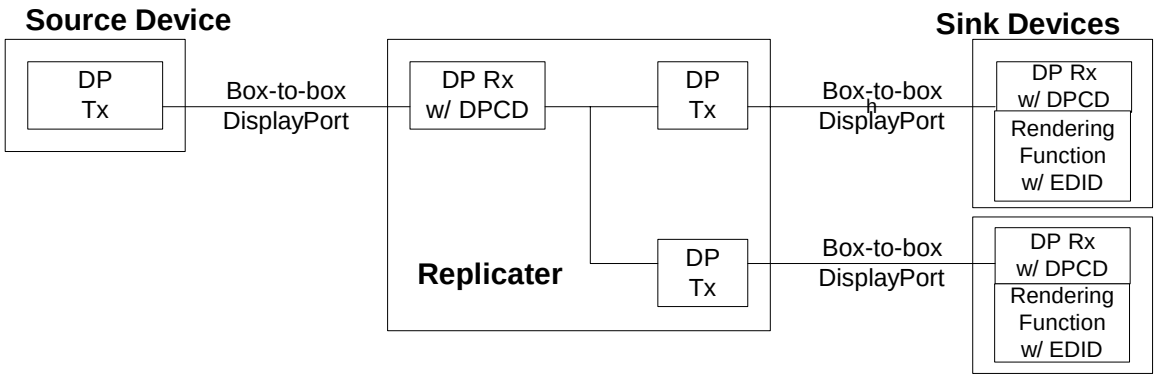



**Figure 2.7 Source Device to Multiple Sink Devices via Replicater**

### *2.1.4.1 EDID and DPCD of Branch Devices*

Upon EDID read by Source Device, Branch Device shall reply with EDID of downstream Sink Device.

As far as the DPCD Receiver Capability is concerned, Branch Device shall update its Receiver Capability field to comprehend not only its own DPCD but also the downstream DPCD.

For example, even if Repeater Device is capable of supporting up to 4 lanes of Main Link, it reports 2-lane support to Source Device if its downstream link is capable of only up to 2 lanes.

#### 2.1.4.1.1 EDID and DPCD Access Handling by Replicater Device (INFORMATIVE)

How Replicater Device handles EDID and DPCD access by an upstream device is implementation specific. For example, Replicater Device may reply with the EDID of Sink Device connected to Downstream Port 0. When such an approach is taken, Replicater Device "NACK's" the EDID read over AUX CH when no device is connected to Downstream Port 0, even if Sink Devices are connected to other downstream ports. In the same token, Replicater Device may use the DPCD of the downstream link of Downstream Port 0. With this approach, Sink Devices connected to downstream ports of Replicater Device other than Downstream Port 0 may be unable to properly receive and/or sink the incoming stream. It is the responsibility of a Replicater Device manufacturer to describe this restriction to a user (in a user's manual and/or with labeling).

#### 2.1.4.1.2 EDID and DPCD Access Handling by Composite Device (INFORMATIVE)

Handling of EDID and DPCD access of by Composite Device is implementation specific. For example, it may reply with EDID of its own Sink and may choose not to comprehend the DPCD of its downstream link.

### *2.1.4.2 Docking Station*

Docking Station is either Replicater Device or Composite Device (with format-converting function) embedded in Source Device. Since it is embedded, the management policy is implementation specific and beyond the scope of this specification. DisplayPort AUX CH address space of 00300h - 003FFh is reserved for vendor-specific usage for Source Device. For example, this address space may be used for configuring a Docking Station.

## *2.2 Isochronous Transport Services*

The isochronous transport services of the Link Layer provide the following.

- Mapping of stream data to and from Main Link lanes
  - Packing/unpacking
  - Stuffing/un-stuffing
  - Framing/un-framing
  - Inter-lane skewing and de-skewing
- Stream clock recovery
- Insertion of Main Stream Attributes data
- Optional insertion secondary-data packet with ECC
  - Audio stream packet
  - CEA861-C InfoFrame packet

### 2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

The Main Link shall have either one, two, or four lanes, with each lane capable of transporting 8 bits of data per link symbol clock (LS_Clk). Main Stream data (namely, an uncompressed video stream) shall be packed, stuffed, framed, and optionally multiplexed with secondary data, and inter-lane skewed before it is handed over to the PHY layer after the link layer data mapping for transport over the Main Link. The stream data shall enter the Link Layer at the original stream clock (Strm_Clk) rate and shall be delivered to PHY layer at LS_Clk rate after this mapping.

Figure 2.8 and Figure 2.9 are the diagrams showing the data mapping in Source and Sink Devices, respectively. Note that these diagrams are logical representations only. Actual implementation is beyond the scope of this specification.

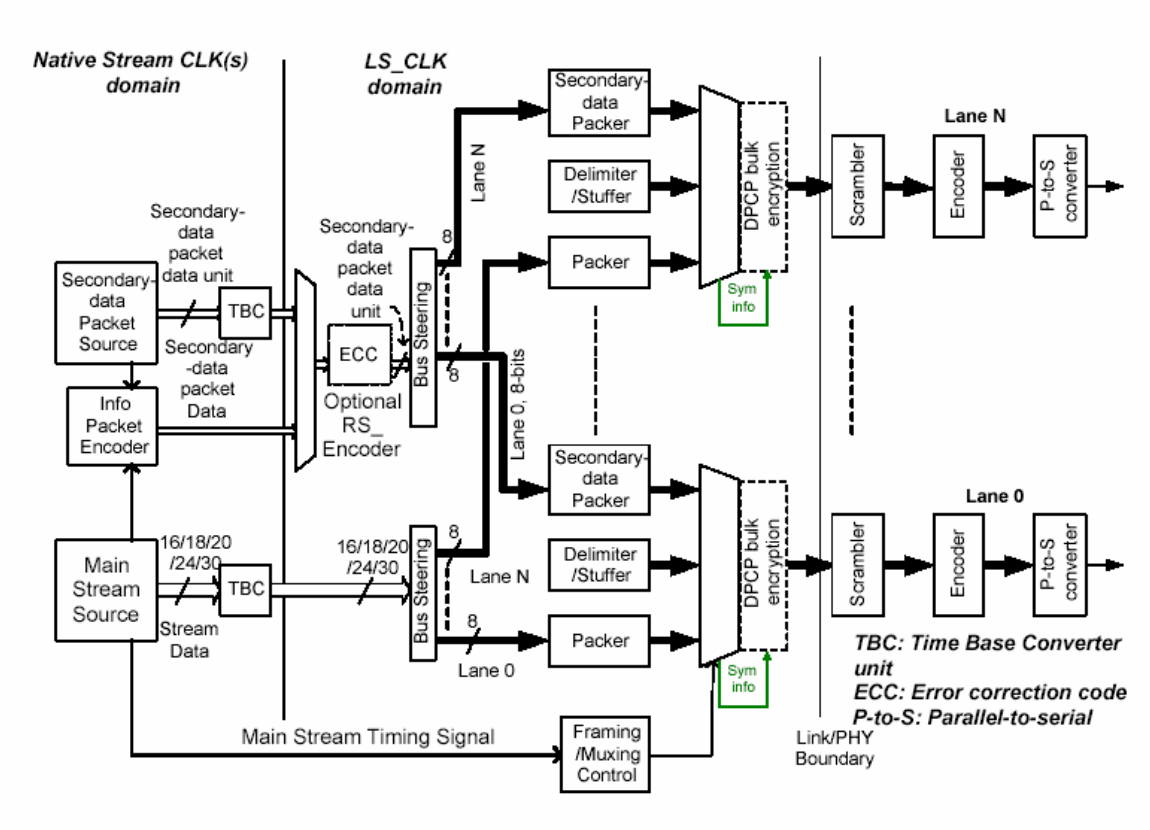



**Figure 2.8 High-level Block Diagram of Transmitter Main Link Data Path**

**Note 1**: Logical block diagram. Actual implementation may vary.
**Note 2**: Both ECC block and DPCP bulk encryption block are optional.

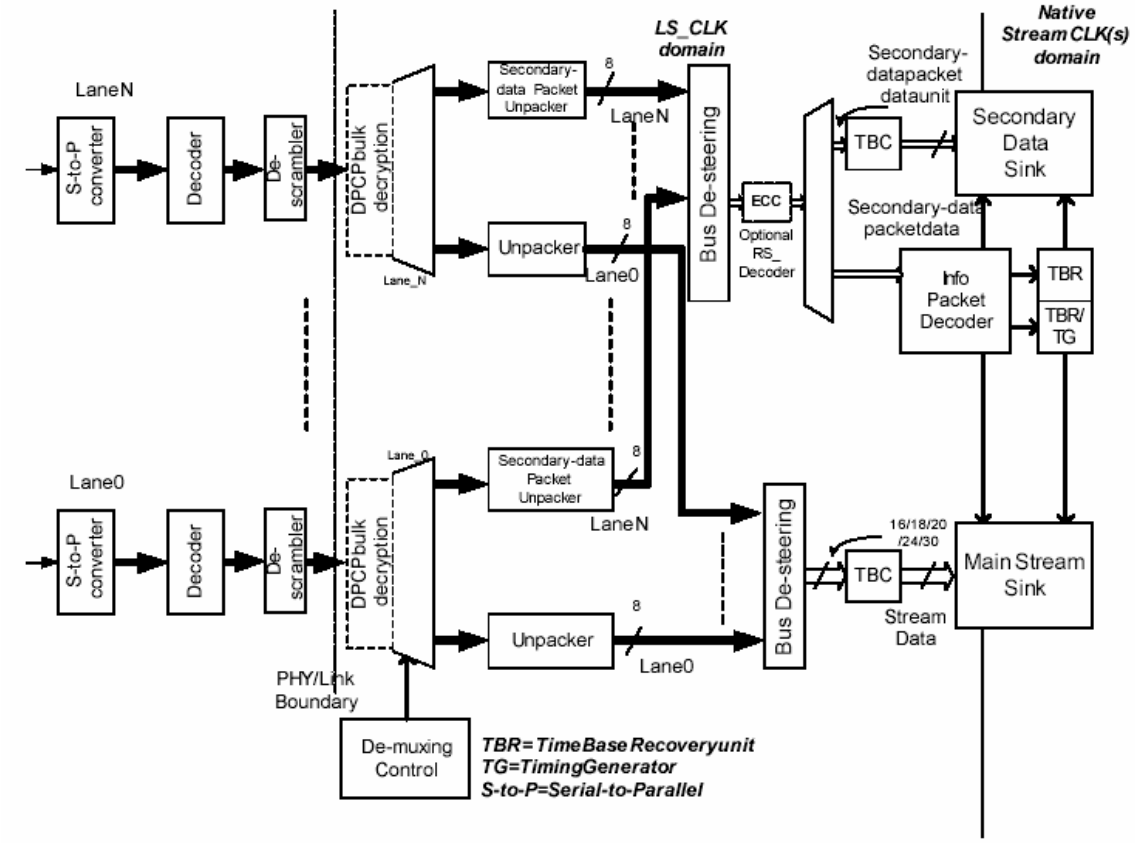



**Figure 2.9 High-level Block Diagram of Receiver Main Link Data Path**

**Note 1**: Logical block diagram. Actual implementation may vary.
**Note 2**: Both ECC block and DPCP bulk decryption block are optional.

Main Link data mapping shall take place in the following order:

- Main Stream data packing, stuffing, and framing
- Optional secondary data framing and multiplexing

### *2.2.1.1 Control Symbols for Framing*

For framing data, the following seven control symbols shall be used:

- BS (Blanking Start)
  - Inserted after the last active pixel during vertical display period.
  - Inserted at the same symbol time during vertical blanking period as during vertical display.
  - This framing symbol shall be periodically (every $2^{13}$ or 8,192 symbols) inserted for active links with no main video stream data to send. In this condition, the BS symbol is immediately followed by VB-ID with its NoVideoStream_Flag set to 1. (For more information on VB-ID, refer to Table 2.2 on p.38.) This link symbol pattern is referred to as “Idle Pattern”.
- BE (Blanking End)
  - Inserted right before the first active pixel of a line only during vertical display period

- FS (Fill Start)
  - Inserted at the beginning of stuffing symbols in Transfer Unit. (Note: Transfer Unit is described in Section 2.2.1.3.1 on p.55.
  - Omitted when there is only one stuffing symbol. FE (Fill End) is inserted without FS in this case.
  - FS and FE are inserted with no stuffing data symbols in between when there are only two stuffing symbols.
- FE (Fill End)
  - Inserted at the end of stuffing symbols within Transfer Unit.
- SS (Secondary-data Start)
  - Inserted at the beginning of secondary data
- SE (Secondary-data End)
  - Inserted at the end of the secondary data
- SR (Scrambler Reset)
  - Every 512th BS symbol shall be replaced with SR symbol by the Physical Layer of the Source Device for resetting the LFSR of the scrambler.
- CPBS (Content Protection BS)
  - Used by DPCP. Refer to APPENDIX 1 on p.204 regarding the usage of CPBS symbol by DPCP.
- CPSR (Content Protection SR)
  - Used by DPCP. Refer to APPENDIX 1 on p.204 regarding the usage of CPSR symbol by DPCP.

These control symbols shall be inserted in all lanes in the same LS_Clk cycle (before they get inter-lane skewed by 2 LS_Clk cycles just before going to the PHY Layer). Link Layer shall distinguish these control symbols from data symbols so that the Physical Layer can properly encode these control symbols using "special characters" different from data characters.

For example, Link Layer may use 9th bit to indicate whether the accompanying 8-bit data represents control symbols or data symbols. There are many ways for Link Layer to implement this distinction. Method used is implementation-specific, and is beyond the scope of this document.

### *2.2.1.2 Main Video Stream Data Packing*

The Link Layer shall first steer pixel data in a pixel-within-lane manner as shown in Table 2.1.

**Table 2.1 Pixel-steering into Main Link Lanes**

| Number of Lanes | Pixel Steering (N is 0 or positive integer) |
|---|---|
| 4 | Pixel 4N to Lane 0<br>Pixel 4N+1 to Lane 1<br>Pixel 4N+2 to Lane 2<br>Pixel 4N+3 to Lane 3 |
| 2 | Pixel 2N to Lane 0<br>Pixel 2N+1 to Lane 1 |
| 1 | All pixels to Lane 0 |

This rule shall apply regardless of the color space/pixel bit depth of the video stream. As shown in Figure 2.10, the first set of active partial pixel data of a line shall follow the control symbol, BE.

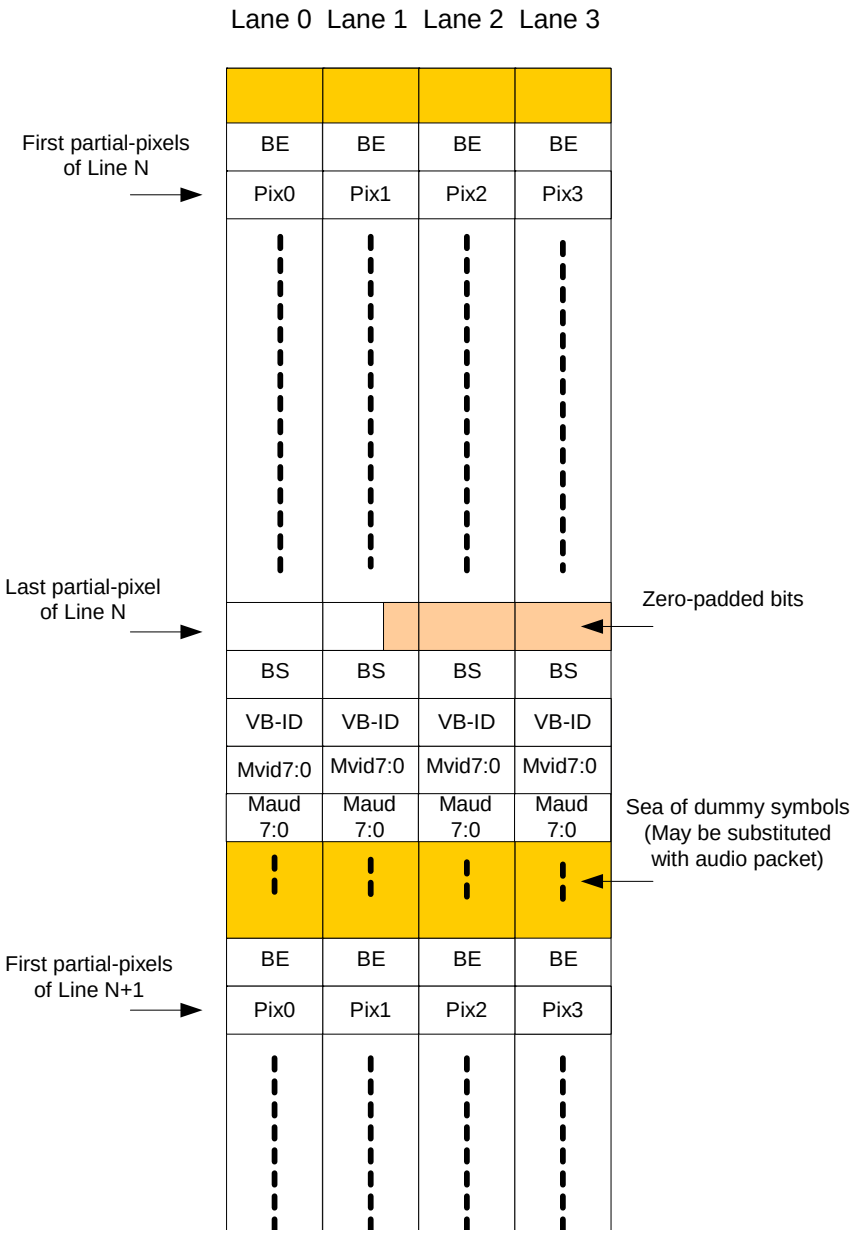



**Figure 2.10 Main Video Stream Data Packing Example for 4 lane Main Link**

**Note**: When there is no audio stream transported, Maud7:0 shall be set to 00h. When there is no video stream transported, Mvid7:0 shall be set to 00h.

During the last symbol time for a line of pixel data, there may be insufficient pixel data to provide data on all lanes of the link. The DisplayPort transmitter shall send zeros for those bits (zero-padded bits).

Immediately following the last symbol period of a line of data the control symbol, BS shall be inserted on all lanes of the link.

The Sink Device, knowing the number of active pixels per horizontal line (via Main Stream Attribute), shall discard zero-padded bits as "don't care."

As can be seen in Figure 2.10, a new line always shall start with Pixel 0 on Lane 0 following BE.

The BS shall be followed on all lanes by VB-ID, Mvid7:0, and Maud7:0.

- VB-ID shall carry the following information:
  - Whether main video stream is in vertical display period or vertical blanking period.
  - Whether main video stream is in odd field or even field for interlaced video
  - Whether the main video stream is interlaced or non-interlaced (progressive)
  - Whether the BS is inserted while no video stream is being transported. The symbols transmitted over the Main Link when with no video stream are shown in Figure 2.11.
  - Whether to mute the audio

**Table 2.2 VB-ID Bit Definition**

| VB-ID Bit | Bit Name | Bit Definition |
|---|---|---|
| Bit 0 | VerticalBlanking_Flag | This bit shall be set to 1 at the end of the last active line and stay 1 during the vertical blanking period. This bit is also set to 1 when there is no video stream (as indicated by Bit 3 set to 1). |
| Bit 1 | FieldID_Flag | This bit shall be set to 0 in even field and to 1 in odd field for interlaced video. For non-interlaced video or no video, this bit shall stay 0. |
| Bit 2 | Interlace_Flag | This bit shall be set to 1 when the main stream is an interlaced video. For non-interlaced video or no video, this bit shall stay 0. |
| Bit 3 | NoVideoStream_Flag | This bit shall be set to 1 when preceding BS is inserted while no video stream is transported. When this bit = 1, the Mvid7:0 value shall be "don't care."<br>Audio stream may be transported even when no main video stream is being transported. |
| Bit 4 | AudioMute_Flag | This bit shall be set to 1 when the audio is to be muted. |
| Bits7:5 | RESERVED | Reserved (All 0's) |

- Mvid7:0

- Least significant 8 bits of time stamp value M for video stream. When there is no video stream transported, set to 00h. (Time stamp shall be used for stream clock recovery, the subject of which is covered in Section 2.2.3 of this chapter.)

- Maud7:0
  - Least significant 8 bits of time stamp value M for audio stream. When there is no audio stream transported, set to 00h.

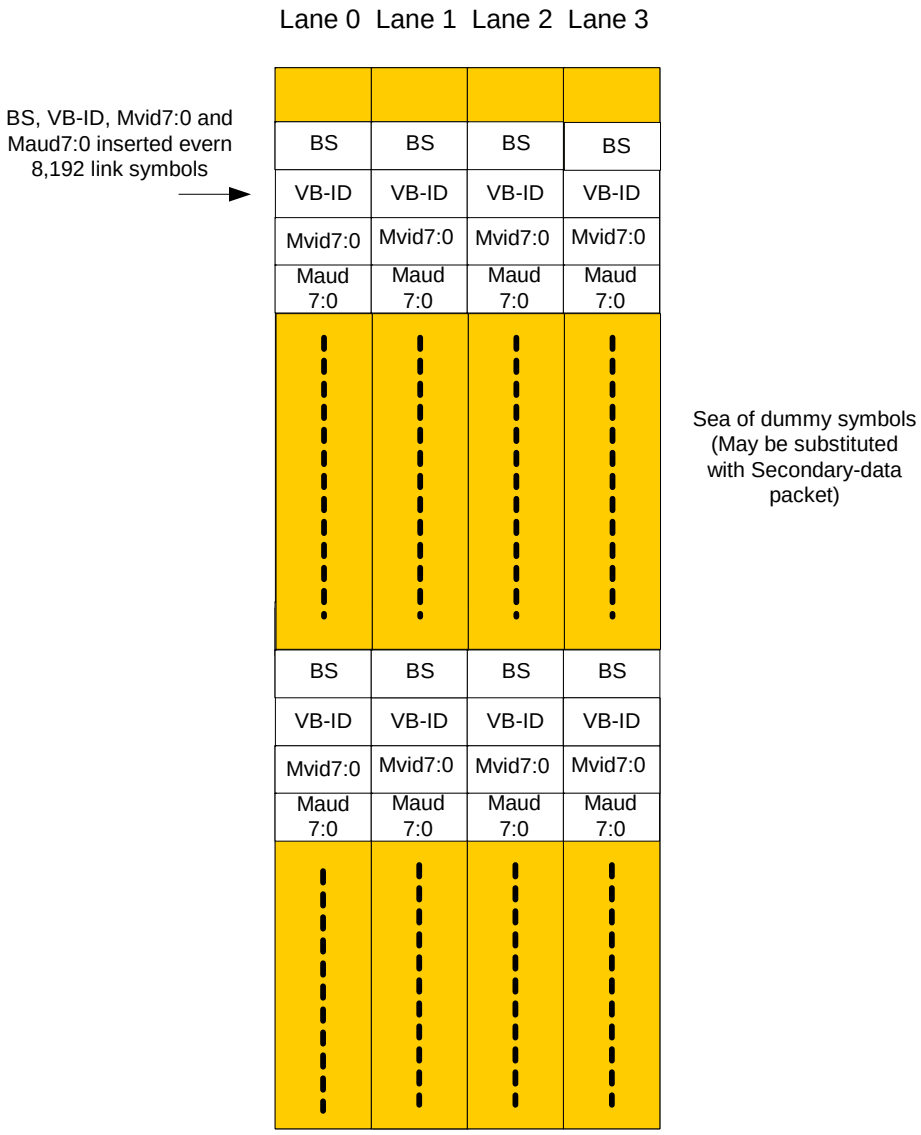



**Figure 2.11 Link Symbols over Main Link without Main Video Stream**

**Note**: Mvid7:0 shall be set to 00h. When there is no audio stream transported, Maud7:0 shall be set to 00h.

The VB-ID, Mvid7:0 and Maud7:0 shall be transported four times, regardless of the number of lanes included in Main Link as shown in Figure 2.12.

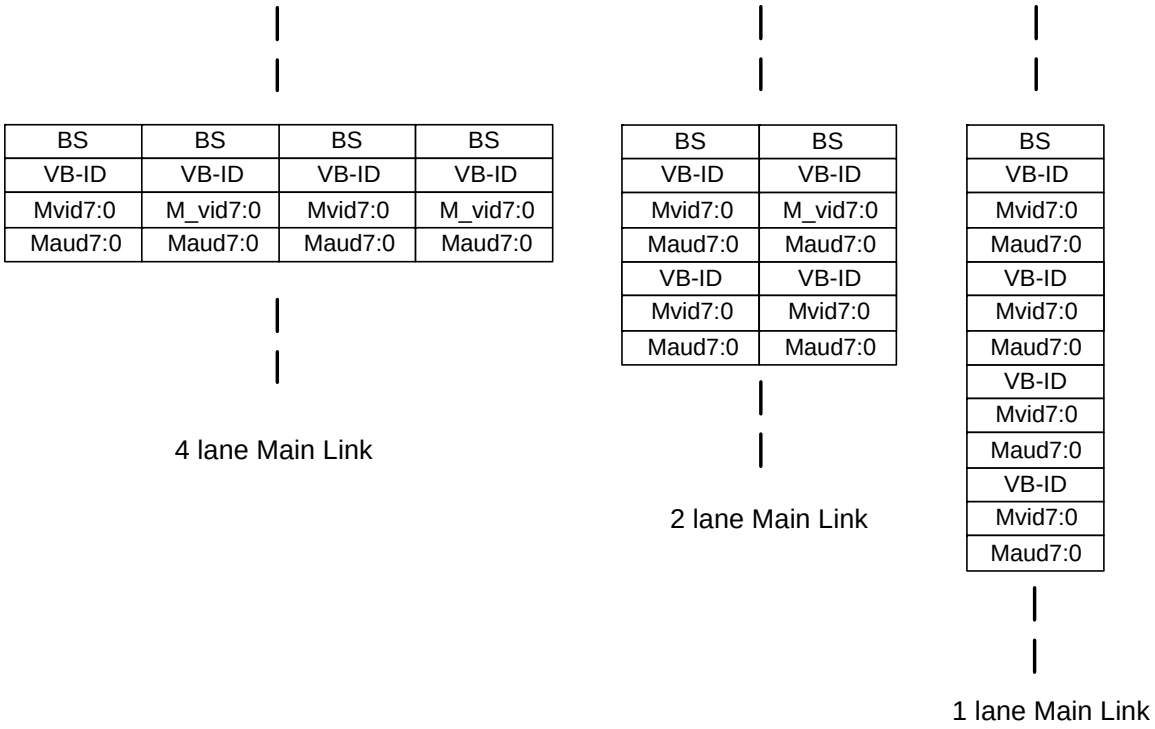



**Figure 2.12 VB-ID/Mvid7:0/Maud7:0 packing over Main Link**

**Note**: If there is no audio stream, Maud7:0 shall be set to 00h. If there is no video stream, Mvid7:0 shall be set to 00h.

Table 2.3 is an example of how a video stream with resolution of 1366x768 and 30 bits-per-pixel (bpp) RGB in color depth is mapped to 4 lanes of Main Link.

**Table 2.3 30-bpp RGB (10 bits per component), 1366x768 packing to 4-lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 | |
|---|---|---|---|---|
| BE | BE | BE | BE | |
| R0-9:2 | R1-9:2 | R2-9:2 | R3-9:2 | <-- Start of Active Pixel |
| R0-1:0\|G0-9:4 | R1-1:0\|G1-9:4 | R2-1:0\|G2-9:4 | R3-1:0\|G3-9:4 | |
| G0-3:0\|B0-9:6 | G1-3:0\|B1-9:6 | G2-3:0\|B2-9:6 | G3-3:0\|B3-9:6 | |
| B0-5:0\|R4-9:8 | B1-5:0\|R5-9:8 | B2-5:0\|R6-9:8 | B3-5:0\|R7-9:8 | |
| R4-7:0 | R5-7:0 | R6-7:0 | R7-7:0 | |
| G4-9:2 | G5-9:2 | G6-9:2 | G7-9:2 | |
| G4-1:0\|B4-9:4 | G5-1:0\|B5-9:4 | G6-1:0\|B6-9:4 | G7-1:0\|B7-9:4 | |
| B4-3:0\|R8-9:6 | B5-3:0\|R9-9:6 | B6-3:0\|R10-9:6 | B7-3:0\|R11-9:6 | |
| R8-5:0\|G8-9:8 | R9-5:0\|G9-9:8 | R10-5:0\|G10-9:8 | R11-5:0\|G11-9:8 | |
| G8-7:0 | G9-7:0 | G10-7:0 | G11-7:0 | |
| B8-9:2 | B9-9:2 | B10-9:2 | B11-9:2 | |
| B8-1:0\|R12-9:4 | B9-1:0\|R13-9:4 | B10-1:0\|R14-9:4 | B11-1:0\|R15-9:4 | |
| R12-3:0\|G12-9:6 | R13-3:0\|G13-9:6 | R14-3:0\|G14-9:6 | R15-3:0\|G15-9:6 | |
| G12-5:0\|B12-9:8 | G13-5:0\|B13-9:8 | G14-5:0\|B14-9:8 | G15-5:0\|B15-9:8 | |
| B12-7:0 | B13-7:0 | B14-7:0 | B15-7:0 | |
| ---------- | ---------- | ---------- | ---------- | |
| R1360-9:2 | R1361-9:2 | R1362-9:2 | R1363-9:2 | |
| R1360-1:0\|G1360-9:4 | R1361-1:0\|G1361-9:4 | R1362-1:0\|G1362-9:4 | R1363-1:0\|G1363-9:4 | |
| G1360-3:0\|B1360-9:6 | G1361-3:0\|B1361-9:6 | G1362-3:0\|B1362-9:6 | G1363-3:0\|B1363-9:6 | |
| B1360-5:0\|R1364-9:8 | B1361-5:0\|R1365-9:8 | B1362-5:0\|--- | B1363-5:0\|--- | |
| R1364-7:0 | R1365-7:0 | --- | --- | |
| G1364-9:2 | G1365-9:2 | --- | --- | |
| G1364-1:0\|B1364-9:4 | G1365-1:0\|B1365-9:4 | --- | --- | |
| B1364-3:0\|--- | B1365-3:0\|--- | --- | --- | |
| BS | BS | BS | BS | <-- End of Active Pixel |
| VB-ID | VB-ID | VB-ID | VB-ID | |
| Mvid7:0 | Mvid7:0 | Mvid7:0 | Mvid7:0 | |
| Maud7:0 | Maud7:0 | Maud7:0 | Maud7:0 | |

**Note 1**: One row of data is transmitted per LS_Clk cycle. Transmitter shall send 0's for "---" in the table.

**Note 2**: R0-9:2 = Red bits 9:2 of pixel, G = Green, B = Blue, BS = Blanking Start, BE = Blanking End. BE = Blanking End. BS = Blanking Start. VB-ID = Video Blanking ID. Mvid7:0 and Maud7:0 are portion of the time stamps for video and audio stream clocks.

The following sub-sections show how 24, 18, 30 bit RGB pixels and 16-/20-24-bit YCbCr422 pixels are mapped into 4, 2, 1 lane Main Link.

As can be seen in Table 2.4 - Table 2.30, when only one lane is enabled of either a 2-lane or a 4-lane DisplayPort device, Lane 0 shall be enabled. When only two lanes are enabled, Lane 0 and Lane 1 shall be enabled.

#### 2.2.1.2.1 24-bpp RGB/YCbCr444 (8 bits per component)

The 24-bpp RGB/YCbCr444 stream mapping into 4, 2, 1-lane Main Link is shown in Table 2.4 - Table 2.6.

**Table 2.4 24-bpp RGB to 4-lane Main Link mapping**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| R0-7:0 | R1-7:0 | R2-7:0 | R3-7:0 |
| G0-7:0 | G1-7:0 | G2-7:0 | G3-7:0 |
| B0-7:0 | B1-7:0 | B2-7:0 | B3-7:0 |
| R4-7:0 | R5-7:0 | R6-7:0 | R7-7:0 |
| G4-7:0 | G5-7:0 | G6-7:0 | G7-7:0 |
| B4-7:0 | B5-7:0 | B6-7:0 | B7-7:0 |
| R8-7:0 | R9-7:0 | R10-7:0 | R11-7:0 |
| G8-7:0 | G9-7:0 | G10-7:0 | G11-7:0 |
| B8-7:0 | B9-7:0 | B10-7:0 | B11-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.5 24-bpp RGB Mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| R0-7:0 | R1-7:0 |
| G0-7:0 | G1-7:0 |
| B0-7:0 | B1-7:0 |
| R2-7:0 | R3-7:0 |
| G2-7:0 | G3-7:0 |
| B2-7:0 | B3-7:0 |
| R4-7:0 | R5-7:0 |
| G4-7:0 | G5-7:0 |
| B4-7:0 | B5-7:0 |
| R6-7:0 | R7-7:0 |
| G6-7:0 | G7-7:0 |
| B6-7:0 | B7-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.6 24-bpp RGB Mapping to 1-lane Main Link**

| Lane 0 |
|---|
| R0-7:0 |
| G0-7:0 |
| B0-7:0 |
| R1-7:0 |
| G1-7:0 |
| B1-7:0 |
| R2-7:0 |
| G2-7:0 |
| B2-7:0 |
| R3-7:0 |
| G3-7:0 |
| B3-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

#### 2.2.1.2.2 18-bpp RGB (6 bits per component)

The 18-bpp RGB stream mapping into 4, 2, and 1 lane Main Link is shown in Table 2.7 - Table 2.9.

**Table 2.7 18-bpp RGB mapping to 4-lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| R0-5:0\|G0-5:4 | R1-5:0\|G1-5:4 | R2-5:0\|G2-5:4 | R3-5:0\|G3-5:4 |
| G0-3:0\|B0-5:2 | G1-3:0\|B1-5:2 | G2-3:0\|B2-5:2 | G3-3:0\|B3-5:2 |
| B0-1:0\|R4-5:0 | B1-1:0\|R5-5:0 | B2-1:0\|R6-5:0 | B3-1:0\|R7-5:0 |
| G4-5:0\|B4-5:4 | G5-5:0\|B5-5:4 | G6-5:0\|B6-5:4 | G7-5:0\|B7-5:4 |
| B4-3:0\|R8-5:2 | B5-3:0\|R9-5:2 | B6-3:0\|R9-5:2 | B7-3:0\|R11-5:2 |
| R8-1:0\|G8-5:0 | R9-1:0\|G9-5:0 | R10-1:0\|G10-5:0 | R11-1:0\|G11-5:0 |
| B8-5:0\|R12-5:4 | B9-5:0\|R13-5:4 | B10-5:0\|R14-5:4 | B11-5:0\|R15-5:4 |
| R12-3:0\|G12-5:2 | R13-3:0\|G13-5:2 | R14-3:0\|G14-5:2 | R15-3:0\|G15-5:2 |
| G12-1:0\|B12-5:0 | G13-1:0\|B13-5:0 | G14-1:0\|B14-5:0 | G15-1:0\|B15-5:0 |

**Table 2.8 18-bpp RGB mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| R0-5:0\|G0-5:4 | R1-5:0\|G1-5:4 |
| G0-3:0\|B0-5:2 | G1-3:0\|B1-5:2 |
| B0-1:0\|R2-5:0 | B1-1:0\|R3-5:0 |
| G2-5:0\|B2-5:4 | G3-5:0\|B3-5:4 |
| B2-3:0\|R4-5:2 | B3-3:0\|R5-5:2 |
| R4-1:0\|G4-5:0 | R5-1:0\|G5-5:0 |
| B4-5:0\|R6-5:4 | B5-5:0\|R7-5:4 |
| R6-3:0\|G6-5:2 | R7-3:0\|G7-5:2 |
| G6-1:0\|B6-5:0 | G7-1:0\|B7-5:0 |

**Table 2.9 18-bpp RGB mapping to 1-lane Main Link**

| Lane 0 |
|---|
| R0-5:0\|G0-5:4 |
| G0-3:0\|B0-5:2 |
| B0-1:0\|R1-5:0 |
| G1-5:0\|B1-5:4 |
| B1-3:0\|R2-5:2 |
| R2-1:0\|G2-5:0 |
| B2-5:0\|R3-5:4 |
| R3-3:0\|G3-5:2 |
| G3-1:0\|B3-5:0 |

#### 2.2.1.2.3 30-bpp RGB/YCbCr444 (10 bits per component)

The 30-bpp RGB/YCbCr444 stream mapping into 4, 2, 1 lane Main Link is shown in Table 2.10 - Table 2.12.

**Table 2.10 30-bpp RGB mapping to 4-lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| R0-9:2 | R1-9:2 | R2-9:2 | R3-9:2 |
| R0-1:0\|G0-9:4 | R1-1:0\|G1-9:4 | R2-1:0\|G2-9:4 | R3-1:0\|G3-9:4 |
| G0-3:0\|B0-9:6 | G1-3:0\|B1-9:6 | G2-3:0\|B2-9:6 | G3-3:0\|B3-9:6 |
| B0-5:0\|R4-9:8 | B1-5:0\|R5-9:8 | B2-5:0\|R6-9:8 | B3-5:0\|R7-9:8 |
| R4-7:0 | R5-7:0 | R6-7:0 | R7-7:0 |
| G4-9:2 | G5-9:2 | G6-9:2 | G7-9:2 |
| G4-1:0\|B49:4 | G5-1:0\|B5-9:4 | G6-1:0\|B6-9:4 | G7-1:0\|B7-9:4 |
| B4-3:0\|R8-9:6 | B5-3:0\|R9-9:6 | B6-3:0\|R10-9:6 | B7-3:0\|R11-9:6 |
| R8-5:0\|G8-9:8 | R9-5:0\|G9-9:8 | R10-5:0\|G10-9:8 | R11-5:0\|G11-9:8 |
| G8-7:0 | G9-7:0 | G10-7:0 | G11-7:0 |
| B8-9:2 | B9-9:2 | B10-9:2 | B11-9:2 |
| B8-1:0\|R12-9:4 | B9-1:0\|R13-9:4 | B10-1:0\|R14-9:4 | B11-1:0\|R15-9:4 |
| R12-3:0\|G12-9:6 | R13-3:0\|G13-9:6 | R14-3:0\|G14-9:6 | R15-3:0\|G15-9:6 |
| G12-5:0\|B12-9:8 | G13-5:0\|B13-9:8 | G14-5:0\|B14-9:8 | G15-5:0\|B15-9:8 |
| B12-7:0 | B13-7:0 | B14-7:0 | B15-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.11 30-bpp RGB mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| R0-9:2 | R1-9:2 |
| R0-1:0\|G0-9:4 | R1-1:0\|G1-9:4 |
| G0-3:0\|B0-9:6 | G1-3:0\|B1-9:6 |
| B0-5:0\|R2-9:8 | B1-5:0\|R3-9:8 |
| R2-7:0 | R3-7:0 |
| G2-9:2 | G3-9:2 |
| G2-1:0\|B2-9:4 | G3-1:0\|B3-9:4 |
| B2-3:0\|R4-9:6 | B3-3:0\|R5-9:6 |
| R4-5:0\|G4-9:8 | R5-5:0\|G5-9:8 |
| G4-7:0 | G5-7:0 |
| B4-9:2 | B5-9:2 |
| B4-1:0\|R6-9:4 | B5-1:0\|R7-9:4 |
| R6-3:0\|G6-9:6 | R7-3:0\|G7-9:6 |
| G6-5:0\|B6-9:8 | G7-5:0\|B7-9:8 |
| B6-7:0 | B7-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.12 30-bpp RGB mapping to 1-lane Main Link**

| Lane 0 |
|---|
| R0-9:2 |
| R0-1:0\|G0-9:4 |
| G0-3:0\|B0-9:6 |
| B0-5:0\|R1-9:8 |
| R1-7:0 |
| G1-9:2 |
| G1-1:0\|B1-9:4 |
| B1-3:0\|R2-9:6 |
| R2-5:0\|G2-9:8 |
| G2-7:0 |
| B2-9:2 |
| B2-1:0\|R3-9:4 |
| R3-3:0\|G3-9:6 |
| G3-5:0\|B3-9:8 |
| B3-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

#### 2.2.1.2.4 36-bpp RGB/YCbCr444 (12 bits per component)

The 36-bpp RGB/YCbCr444 stream mapping into 4-/2-/1-lane Main Link is shown in Table 2.13 - Table 2.15.

**Table 2.13 36-bpp RGB to 4-lane Main Link mapping**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| R0-11:4 | R1-11:4 | R2-11:4 | R3-11:4 |
| R0-3:0\|G0-11:8 | R1-3:0\|G1-11:8 | R2-3:0\|G2-11:8 | R3-3:0\|G3-11:8 |
| G0-7:0\|B0-11:8 | G1-7:0\|B1-11:8 | G2-7:0\|B2-11:8 | G3-7:0\|B3-11:8 |
| B0-7:0 | B1-7:0 | B2-7:0 | B3-7:0 |
| R4-11:4 | R5-11:4 | R6-11:4 | R7-11:4 |
| R4-3:0\|G4-11:8 | R5-3:0\|G5-11:8 | R6-3:0\|G6-11:8 | R7-3:0\|G7-11:8 |
| G4-7:0\|B4-11:8 | G5-7:0\|B5-11:8 | G6-7:0\|B6-11:8 | G7-7:0\|B7-11:8 |
| B4-7:0 | B5-7:0 | B6-7:0 | B7-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.14 36-bpp RGB Mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| R0-11:4 | R1-11:4 |
| R0-3:0\|G0-11:8 | R1-3:0\|G1-11:8 |
| G0-7:0\|B0-11:8 | G1-7:0\|B1-11:8 |
| B0-7:0 | B1-7:0 |
| R2-11:4 | R3-11:4 |
| R2-3:0\|G2-11:8 | R3-3:0\|G3-11:8 |
| G2-7:0\|B2-11:8 | G3-7:0\|B3-11:8 |
| B2-7:0 | B3-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.15 36-bpp RGB Mapping to 1-lane Main Link**

| Lane 0 |
|---|
| R0-11:4 |
| R0-3:0\|G0-11:8 |
| G0-7:0\|B0-11:8 |
| B0-7:0 |
| R1-11:4 |
| R1-3:0\|G1-11:8 |
| G1-7:0\|B1-11:8 |
| B1-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

#### 2.2.1.2.5 48-bpp RGB/YCbCr444 (16 bits per component)

The 48-bpp RGB/YCbCr444 stream mapping into 4-/2-/1-lane Main Link is shown in Table 2.16 - Table 2.18.

**Table 2.16 48-bpp RGB to 4-lane Main Link mapping**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| R0-15:8 | R1-15:8 | R2-15:8 | R3-15:8 |
| R0-7:0 | R1-7:0 | R2-7:0 | R3-7:0 |
| G0-15:8 | G1-15:8 | G2-15:8 | G3-15:8 |
| G0-7:0 | G1-7:0 | G2-7:0 | G3-7:0 |
| B0-15:8 | B1-15:8 | B2-15:8 | B3-15:8 |
| B0-7:0 | B1-7:0 | B2-7:0 | B3-7:0 |
| R4-15:8 | R5-15:8 | R6-15:8 | R7-15:8 |
| R4-7:0 | R5-7:0 | R6-7:0 | R7-7:0 |
| G4-15:8 | G5-15:8 | G6-15:8 | G7-15:8 |
| G4-7:0 | G5-7:0 | G6-7:0 | G7-7:0 |
| B4-15:8 | B5-15:8 | B6-15:8 | B7-15:8 |
| B4-7:0 | B5-7:0 | B6-7:0 | B7-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.17 48-bpp RGB Mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| R0-15:8 | R1-15:8 |
| R0-7:0 | R1-7:0 |
| G0-15:8 | G1-15:8 |
| G0-7:0 | G1-7:0 |
| B0-15:8 | B1-15:8 |
| B0-7:0 | B1-7:0 |
| R2-15:8 | R3-15:8 |
| R2-7:0 | R3-7:0 |
| G2-15:8 | G3-15:8 |
| G2-7:0 | G3-7:0 |
| B2-15:8 | B3-15:8 |
| B2-7:0 | B3-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

**Table 2.18 48-bpp RGB Mapping to 1-lane Main Link**

| Lane 0 |
|---|
| R0-15:8 |
| R0-7:0 |
| G0-15:8 |
| G0-7:0 |
| B0-15:8 |
| B0-7:0 |
| R1-15:8 |
| R1-7:0 |
| G1-15:8 |
| G1-7:0 |
| B1-15:8 |
| B1-7:0 |

**Note**: For YCbCr444, replace R with Cr, G with Y, and B with Cb.

#### 2.2.1.2.6 16-bpp YCbCr422 (8 bits per component)

The 16-bpp YCbCr422 stream mapping into 4, 2, 1 lane Main Link is shown in Table 2.19 - Table 2.21.

**Table 2.19 16-bpp YCbCr422 mapping to 4-lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| Cb0-7:0 | Cb2-7:0 | Cb4-7:0 | Cb6-7:0 |
| Y0-7:0 | Y2-7:0 | Y4-7:0 | Y6-7:0 |
| Cr0-7:0 | Cr2-7:0 | Cr4-7:0 | Cr6-7:0 |
| Y1-7:0 | Y3-7:0 | Y5-7:0 | Y7-7:0 |
| Cb8-7:0 | Cb10-7:0 | Cb12-7:0 | Cb14-7:0 |
| Y8-7:0 | Y10-7:0 | Y12-7:0 | Y14-7:0 |
| Cr8-7:0 | Cr10-7:0 | Cr12-7:0 | Cr14-7:0 |
| Y9-7:0 | Y11-7:0 | Y13-7:0 | Y15-7:0 |
| Cb16-7:0 | Cb18-7:0 | Cb20-7:0 | Cb22-7:0 |
| Y16-7:0 | Y18-7:0 | Y20-7:0 | Y22-7:0 |
| Cr16-7:0 | Cr18-7:0 | Cr20-7:0 | Cr22-7:0 |
| Y17-7:0 | Y19-7:0 | Y21-7:0 | Y23-7:0 |

**Table 2.20 16-bpp YCbCr422 mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| Cb0-7:0 | Cb2-7:0 |
| Y0-7:0 | Y2-7:0 |
| Cr0-7:0 | Cr2-7:0 |
| Y1-7:0 | Y3-7:0 |
| Cb4-7:0 | Cb6-7:0 |
| Y4-7:0 | Y6-7:0 |
| Cr4-7:0 | Cr6-7:0 |
| Y5-7:0 | Y7-7:0 |
| Cb8-7:0 | Cb10-7:0 |
| Y8-7:0 | Y10-7:0 |
| Cr8-7:0 | Cr10-7:0 |
| Y9-7:0 | Y11-7:0 |

**Table 2.21 16-bpp YCbCr422 mapping to 1-lane Main Link**

| Lane 0 |
|---|
| Cb0-7:0 |
| Y0-7:0 |
| Cr0-7:0 |
| Y1-7:0 |
| Cb2-7:0 |
| Y2-7:0 |
| Cr2-7:0 |
| Y3-7:0 |
| Cb4-7:0 |
| Y4-7:0 |
| Cr4-7:0 |
| Y5-7:0 |

#### 2.2.1.2.7 20-bpp YCbCr422 (10 bits per component)

The 20-bpp YCbCr422 stream mapping into 4, 2, 1 lane Main Link is shown in Table 2.22 - Table 2.24.

**Table 2.22 20-bpp YCbCr422 mapping to 4-lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| Cb0-9:2 | Cb2-9:2 | Cb4-9:2 | Cb6-9:2 |
| Cb0-1:0\|Y0-9:4 | Cb2-1:0\|Y2-9:4 | Cb4-1:0\|Y4-9:4 | Cb6-1:0\|Y6-9:4 |
| Y0-3:0\|Cr0-9:6 | Y2-3:0\|Cr2-9:6 | Y4-3:0\|Cr4-9:6 | Y6-3:0\|Cr6-9:6 |
| Cr0-5:0\|Y1-9:8 | Cr2-5:0\|Y3-9:8 | Cr4-5:0\|Y5-9:8 | Cr6-5:0\|Y7-9:8 |
| Y1-7:0 | Y3-7:0 | Y5-7:0 | Y7-7:0 |
| Cb8-9:2 | Cb10-9:2 | Cb12-9:2 | Cb14-9:2 |
| Cb8-1:0\|Y8-9:4 | Cb10-1:0\|Y10-9:4 | Cb12-1:0\|Y12-9:4 | Cb14-1:0\|Y14-9:4 |
| Y8-3:0\|Cr8-9:6 | Y10-3:0\|Cr10-9:6 | Y12-3:0\|Cr12-9:6 | Y14-3:0\|Cr14-9:6 |
| Cr8-5:0\|Y9-9:8 | Cr10-5:0\|Y11-9:8 | Cr12-5:0\|Y13-9:8 | Cr14-5:0\|Y15-9:8 |
| Y9-7:0 | Y11-7:0 | Y13-7:0 | Y15-7:0 |

**Table 2.23 20-bpp YCbCr422 mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| Cb0-9:2 | Cb2-9:2 |
| Cb0-1:0\|Y0-9:4 | Cb2-1:0\|Y2-9:4 |
| Y0-3:0\|Cr0-9:6 | Y2-3:0\|Cr2-9:6 |
| Cr0-5:0\|Y1-9:8 | Cr2-5:0\|Y3-9:8 |
| Y1-7:0 | Y3-7:0 |
| Cb4-9:2 | Cb6-9:2 |
| Cb4-1:0\|Y4-9:4 | Cb6-1:0\|Y6-9:4 |
| Y4-3:0\|Cr4-9:6 | Y6-3:0\|Cr6-9:6 |
| Cr4-5:0\|Y5-9:8 | Cr6-5:0\|Y7-9:8 |
| Y5-7:0 | Y7-7:0 |

**Table 2.24 20-bpp YCbCr422 mapping to 1-lane Main Link**

| Lane 0 |
|---|
| Cb0-9:2 |
| Cb0-1:0\|Y0-9:4 |
| Y0-3:0\|Cr0-9:6 |
| Cr0-5:0\|Y1-9:8 |
| Y1-7:0 |
| Cb2-9:2 |
| Cb2-1:0\|Y2-9:4 |
| Y2-3:0\|Cr2-9:6 |
| Cr2-5:0\|Y3-9:8 |
| Y3-7:0 |

#### 2.2.1.2.8 24-bpp YCbCr422 (12 bits per component)

The 24-bpp YCbCr422 stream mapping into 4, 2, 1 lane Main Link is shown in Table 2.25 - Table 2.27.

**Table 2.25 24-bpp YCbCr422 mapping to 4-lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| Cb0-11:4 | Cb2-11:4 | Cb4-11:4 | Cb6-11:4 |
| Cb0-3:0\|Y0-11:8 | Cb2-3:0\|Y2-11:8 | Cb4-3:0\|Y4-11:8 | Cb6-3:0\|Y6-11:8 |
| Y0-7:0 | Y2-7:0 | Y4-7:0 | Y6-7:0 |
| Cr0-11:4 | Cr2-11:4 | Cr4-11:4 | Cr6-11:4 |
| Cr0-3:0\|Y1-11:8 | Cr2-3:0\|Y3-11:8 | Cr4-3:0\|Y5-11:8 | Cr6-3:0\|Y7-11:8 |
| Y1-7:0 | Y3-7:0 | Y5-7:0 | Y7-7:0 |

**Table 2.26 24-bpp YCbCr422 mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| Cb0-11:4 | Cb2-11:4 |
| Cb0-3:0\|Y0-11:8 | Cb2-3:0\|Y2-11:8 |
| Y0-7:0 | Y2-7:0 |
| Cr0-11:4 | Cr2-11:4 |
| Cr0-3:0\|Y1-11:8 | Cr2-3:0\|Y3-11:8 |
| Y1-7:0 | Y3-7:0 |

**Table 2.27 24-bpp YCbCr422 mapping to 1-lane Main Link**

| Lane 0 |
|---|
| Cb0-11:4 |
| Cb0-3:0\|Y0-11:8 |
| Y0-7:0 |
| Cr0-11:4 |
| Cr0-3:0\|Y1-11:8 |
| Y1-7:0 |

#### 2.2.1.2.9 32-bpp YCbCr422 (16 bits per component)

The 32-bpp YCbCr422 stream mapping into 4, 2, 1 lane Main Link is shown in Table 2.28 - Table 2.30.

**Table 2.28 32-bpp YCbCr422 mapping to 4-lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| Cb0-15:8 | Cb2-15:8 | Cb4-15:8 | Cb6-15:8 |
| Cb0-7:0 | Cb2-7:0 | Cb4-7:0 | Cb6-7:0 |
| Y0-15:8 | Y2-15:8 | Y4-15:8 | Y6-15:8 |
| Y0-7:0 | Y2-7:0 | Y4-7:0 | Y6-7:0 |
| Cr0-15:8 | Cr2-15:8 | Cr4-15:8 | Cr6-15:8 |
| Cr0-7:0 | Cr2-7:0 | Cr4-7:0 | Cr6-7:0 |
| Y1-15:8 | Y3-15:8 | Y5-15:8 | Y7-15:8 |
| Y1-7:0 | Y3-7:0 | Y5-7:0 | Y7-7:0 |
| Cb8-15:8 | Cb10-15:8 | Cb12-15:8 | Cb14-15:8 |
| Cb8-7:0 | Cb10-7:0 | Cb12-7:0 | Cb14-7:0 |
| Y8-15:8 | Y10-15:8 | Y12-15:8 | Y14-15:8 |
| Y8-7:0 | Y10-7:0 | Y12-7:0 | Y14-7:0 |
| Cr8-15:8 | Cr10-15:8 | Cr12-15:8 | Cr14-15:8 |
| Cr8-7:0 | Cr10-7:0 | Cr12-7:0 | Cr14-7:0 |
| Y9-15:8 | Y11-15:8 | Y13-15:8 | Y15-15:8 |
| Y9-7:0 | Y11-7:0 | Y13-7:0 | Y15-7:0 |

**Table 2.29 32-bpp YCbCr422 mapping to 2-lane Main Link**

| Lane 0 | Lane 1 |
|---|---|
| Cb0-15:8 | Cb2-15:8 |
| Cb0-7:0 | Cb2-7:0 |
| Y0-15:8 | Y2-15:8 |
| Y0-7:0 | Y2-7:0 |
| Cr0-15:8 | Cr2-15:8 |
| Cr0-7:0 | Cr2-7:0 |
| Y1-15:8 | Y3-15:8 |
| Y1-7:0 | Y3-7:0 |
| Cb4-15:8 | Cb6-15:8 |
| Cb4-7:0 | Cb6-7:0 |
| Y4-15:8 | Y6-15:8 |
| Y4-7:0 | Y6-7:0 |
| Cr4-15:8 | Cr6-15:8 |
| Cr4-7:0 | Cr6-7:0 |
| Y5-15:8 | Y7-15:8 |
| Y5-7:0 | Y7-7:0 |

**Table 2.30 32-bpp YCbCr422 mapping to 1-lane Main Link**

| Lane 0 |
|---|
| Cb0-15:8 |
| Cb0-7:0 |
| Y0-15:8 |
| Y0-7:0 |
| Cr0-15:8 |
| Cr0-7:0 |
| Y1-15:8 |
| Y1-7:0 |
| Cb2-15:8 |
| Cb2-7:0 |
| Y2-15:8 |
| Y2-7:0 |
| Cr2-15:8 |
| Cr2-7:0 |
| Y3-15:8 |
| Y3-7:0 |

### *2.2.1.3 Symbol Stuffing and Transfer Unit*

To avoid the oversubscription of the link bandwidth, the packed-data rate shall be equal to or lower than the link symbol rate. When the packed-data rate is lower than the link symbol rate, Link Layer shall perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) shall be inserted in all lanes in the same LS_Clk cycle before inter-lane skewing.

The way symbols are stuffed shall be different between active video period and blanking period.

- During active video period:
  - Stuffing symbols shall be framed with control symbols FS & FE within Transfer Unit (TU) as shown in Figure 2.13. (TU is described with an example in the next section, Section 2.2.1.3.1.) All the symbols between FS and FE shall be stuffing dummy data symbols, while all the symbols in the TU before FS shall be valid data symbols.
  - FS and FE shall be inserted in all lanes in the same LS_Clk cycle.
  - When there is only one symbol to stuff, FE shall be used and FS is omitted.
  - Transfer Unit size shall be 64 link symbols per lane.
  - The last TU of a horizontal video line shall end with BS and shall not end with FS/FE insertion.
- During blanking period:
  - All symbols in between BS and BE are dummy stuffing data symbols (except for VB-ID, Mvid7:0 and Maud7:0). These dummy data symbols may be substituted with Secondary-data Packets.
  - During vertical blanking period, BS is transmitted on each lane followed by VB-ID, Mvid7:0 and Maud7:0. All the rest of the symbols between the BS at the beginning of vertical blanking interval and the BE at the end of the vertical blanking interval are dummy symbols that may be substituted with Secondary-data Packets.

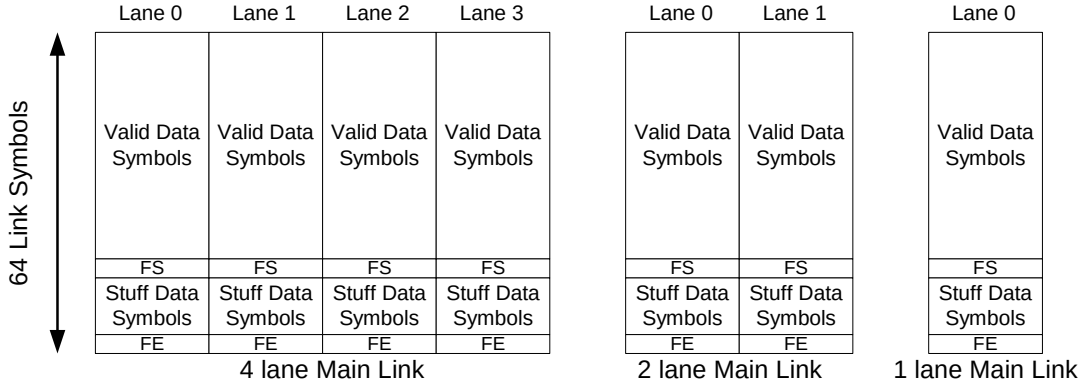



**Figure 2.13 Transfer Unit**

The first pixel data of the horizontal active display line, immediately after BE, shall be placed as the first valid data symbols of the first TU of a line. The partial pixel data of Pixel 0 shall always be placed on Lane 0.

TU may end at a partial pixel boundary. For example, a part of blue data of pixel may be transported in one TU while the rest of the blue data of that pixel is transported in the next TU, as shown in 0.

Source shall equally distribute the valid symbols in each of the TU's (except for the last TU of a line which may be cut because of the end of active pixel). The number of valid data symbols per lane per TU shall follow the equation below:

- # of valid data symbols = packed data rate/link symbol rate * 64

Transfer Unit must have an integer number of valid data symbols. For those cases where the above equation leads to a non-integer result, the actual number of valid data symbols shall vary over time between the integer values immediately above and below the result obtained from the equation, average of which overtime becomes equal to the non-integer number calculated from the equation. (When the valid data symbol count per TU is less than 1, some TUs will have no valid data symbol.)

The last TU at the end of the horizontal active display period may (or is likely to) have fewer valid data symbols than that obtained from the above equation. The DisplayPort receiver shall discard all the data symbols after BS (except for VB-ID, Mvid7:0, and Maud7:0) as well as those "zero-padded bits" at the end of the horizontal active display period.

#### 2.2.1.3.1 Transfer Unit Example (INFORMATIVE)

Table 2.31 shows an example of Transfer Unit for a 1366x768, 30-bpp RGB video stream (Strm_Clk = 80MHz) transported over 4-lane Main Link running at 2.7Gbps (or 270M-symbols per second per lane).

The number of valid symbols within the Transfer Unit is calculated as follows:

- Stream: 30bpp, 80MHz → Packed data rate over 4 lanes = 75Msymbols/sec/lane
- Valid symbols per TU = 75M/270M * 64 = 17.8 → 17 or 18 symbols per lane

The number of valid data symbols per TU will naturally alternate between 17 or 18, and over time, the average number will come to the appropriate non-integer value calculated from the above equation.

**Table 2.31 Transfer Unit of 30-bpp RGB video over 2.7Gbps/lane Main Link**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| BE | BE | BE | BE |
| R0-9:2 | R1-9:2 | R2-9:2 | R3-9:2 |
| R0-1:0\|G0-9:4 | R1-1:0\|G1-9:4 | R2-1:0\|G2-9:4 | R3-1:0\|G3-9:4 |
| G0-3:0\|B0-9:6 | G1-3:0\|B1-9:6 | G2-3:0\|B2-9:6 | G3-3:0\|B3-9:6 |
| B0-5:0\|R4-9:8 | B1-5:0\|R5-9:8 | B2-5:0\|R6-9:8 | B3-5:0\|R7-9:8 |
| R4-7:0 | R5-7:0 | R6-7:0 | R7-7:0 |
| G4-9:2 | G5-9:2 | G6-9:2 | G7-9:2 |
| G4-1:0\|B4-9:4 | G5-1:0\|B5-9:4 | G6-1:0\|B6-9:4 | G7-1:0\|B7-9:4 |
| B4-3:0\|R8-9:6 | B5-3:0\|R9-9:6 | B6-3:0\|R10-9:6 | B7-3:0\|R11-9:6 |
| R8-5:0\|G8-9:8 | R9-5:0\|G9-9:8 | R10-5:0\|G10-9:8 | R11-5:0\|G11-9:8 |
| G8-7:0 | G9-7:0 | G10-7:0 | G11-7:0 |
| B8-9:2 | B9-9:2 | B10-9:2 | B11-9:2 |
| B8-1:0\|R12-9:4 | B9-1:0\|R13-9:4 | B10-1:0\|R14-9:4 | B11-1:0\|R15-9:4 |
| R12-3:0\|G12-9:6 | R13-3:0\|G13-9:6 | R14-3:0\|G14-9:6 | R15-3:0\|G15-9:6 |
| G12-5:0\|B12-9:8 | G13-5:0\|B13-9:8 | G14-5:0\|B14-9:8 | G15-5:0\|B15-9:8 |
| B12-7:0 | B13-7:0 | B14-7:0 | B15-7:0 |
| R16-9:2 | R17-9:2 | R18-9:2 | R19-9:2 |
| R16-1:0\|G16-9:4 | R17-1:0\|G17-9:4 | R18-1:0\|G18-9:4 | R19-1:0\|G19-9:4 |
| G16-3:0\|B16-9:6 | G17-3:0\|B17-9:6 | G18-3:0\|B18-9:6 | G19-3:0\|B19-9:6 |
| FS | FS | FS | FS |
| Dummy Data Symbols (44 x 4) | | | |
| FE | FE | FE | FE |
| B16-5:0\|R20-9:8 | B17-5:0\|R21-9:8 | B18-5:0\|R22-9:8 | B19-5:0\|R23-9:8 |
| R20-7:0 | R21-7:0 | R22-7:0 | R23-7:0 |

---

**Note**: The pixel rate in this example is 80Mpixels per sec. The Main Link bit rate is 2.7Gbps per lane. The first TU of a line is marked by the blue arrow to the right of the table.

As can be seen in the above example, the valid data in a Transfer Unit may end at non-pixel boundary.

### *2.2.1.4 Main Stream Attribute/Secondary-Data Packet Insertion*

The dummy stuffing data symbols during video blanking period (both vertical and horizontal) may be substituted either with Main Stream Attributes data or optional secondary-data packet. Both shall be framed with SS and SE control symbols as shown in Figure 2.14.

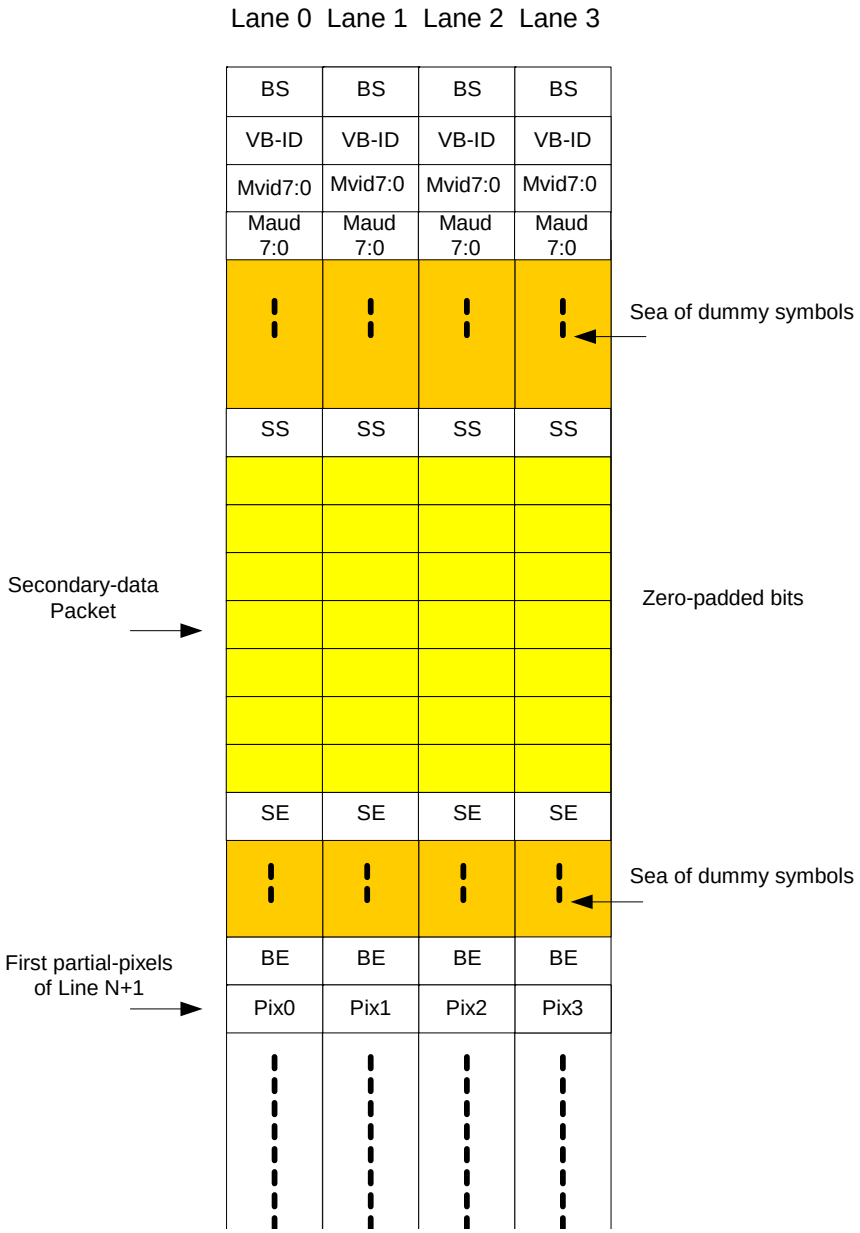



**Figure 2.14 Secondary Data Insertion**

Secondary-data packets are used, for example, for the following purposes:

- CEA861C InfoFrame packet
- Audio stream packet

- Audio time stamp packet

Main Stream Attribute data shall be protected via redundancy. The redundancy shall be further enhanced via inter-lane skewing as described in the next section. Secondary-data packets shall be protected via ECC (error correcting code) based on Reed Solomon code as described in Section 0.

### *2.2.1.5 Inter-lane Skewing*

After inserting Main Link Attributes data (and optionally secondary-data packet), the DisplayPort transmitter shall insert a skew of two LS_Clk cycles between adjacent lanes. Figure 2.15 shows how the symbols shall be transported after this inter-lane skewing. All the symbols, both those transmitted during video display period and those transmitted during video blanking period, are skewed by two LS_Clk period between adjacent lanes.

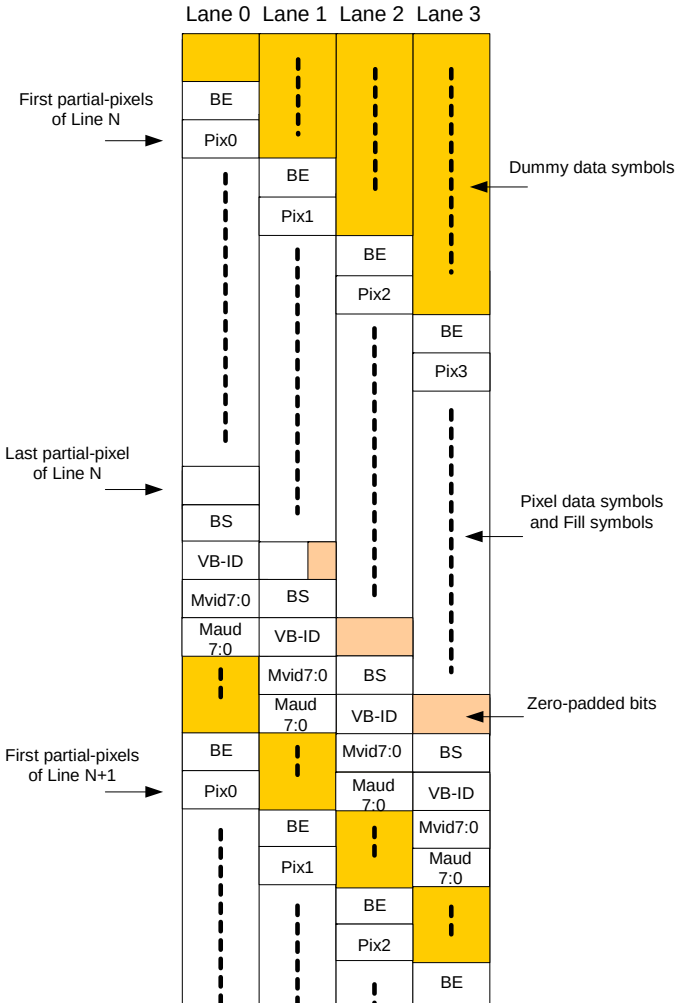



**Figure 2.15 Inter-lane Skewing**

The purpose of the inter-lane skewing is to increase the immunity of the link against external noise. Without inter-lane skewing an external impulse may, for example, corrupt the Mvid7:0 symbols on all lanes. Inter-lane skewing reduces the possibility of such a corruption.

### 2.2.2 Stream Reconstruction in the Sink

The stream reconstruction by the Link Layer in the Sink Device shall be a mirror image of what takes place within the Source Device. The following actions shall be taken by the Sink Device:

- Inter-lane de-skewing

  Shall remove the 2-LS_Clk skewing among adjacent lanes inserted by the transmitter

- Error correction

  All the values of DisplayPort Main Stream Attributes except for Time Stamp Value M shall stay constant over time. Therefore, the DisplayPort receiver shall filter out any intermittent data corruption by comparing with the previous values.

  As for the Time Stamp values Mvid/Maud and VB-ID, “majority voting” shall be used to determine the value.

- Secondary-data packet de-multiplexing

  Secondary data shall be de-multiplexed using SS and SE as the separator.
  The DisplayPort receiver shall perform Reed-Solomon (15, 13) (RS (15, 13)) decoding upon extracting the secondary-data packet.

- Symbol un-stuffing

  Stuffing symbols get removed.

- Data unpacking

  Data unpacking shall take place to reconstruct pixel data from data characters transported over Main Link. Unpacking is dependent on the pixel data color depth and format (as described in Section 2.2.1.2),

- Stream clock recovery

  Stream clock recovery is covered in the next section.

### 2.2.3 Stream Clock Recovery

This section describes the details of original stream clock recovery from Main Link in the Sink Device. The following equations conceptually explain how Stream clock (Strm_Clk) shall be derived from Link Symbol clock (LS_Clk) using Time Stamps, M and N:

- f_Strm_Clk = M/N * f_LS_Clk, where
  - N = Reference pulse period/t_LS_Clk
  - M = Feedback pulse period/t_Strm_Clk

The f_Strm_Clk and the f_LS_Clk are stream clock and link symbol clock frequencies, while the t_Strm_Clk and t_LS_Clk are stream clock and link symbol clock periods, respectively. The reference pulse and feedback pulse are shown in Figure 2.16 below.

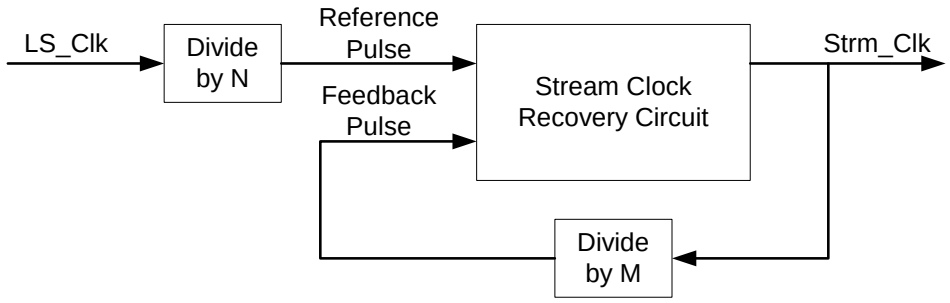



**Figure 2.16 Reference Pulse and Feedback Pulse of Stream Clock Recovery Circuit**

The above equation can also be expressed as:

- M/N = f_Strm_Clk/f_LS_Clk

Both M and N shall be 24-bit values.

When the DisplayPort transmitter and the stream source share the same reference clock, N and M values stay constant. This way of generating link clock and stream clock is called Synchronous Clock mode. DisplayPort Source Device may select a stream clock frequency that allows for a stationary and relatively small (for example, 64 or less) M and N values. These choices are implementation specific.

If the Stream clock and Link Symbol clock are asynchronous with each other, the value of M changes over time. This way of generating link clock and stream clock is called Asynchronous Clock mode. The value M shall change over, while the value N stays constant. The value of N in this Asynchronous Clock mode shall be set to $2^{15}$ or 32,768.

When in Asynchronous Clock mode, the DisplayPort transmitter shall measure M using a counter running at LS_Clk as shown in Figure 2.17. The full counter value after every [N x LS_Clk cycles] shall be transported in the DisplayPort Main Stream Attributes. . The least significant 8 bits of M (Mvid7:0) shall be transported once per main video stream horizontal period following BS and VB-ID.

When Mvid7:0 is either close to 00h or FFh, the change in Mvid7:0 may also change the Mvid23:8. For example, when Mvid23:0 is 000FFFh at one point in time for a given main video stream, the value may turn to 0010000h at another point. Sink Device is responsible for determining the entire Mvid23:0 value based on the updated Mvid7:0.

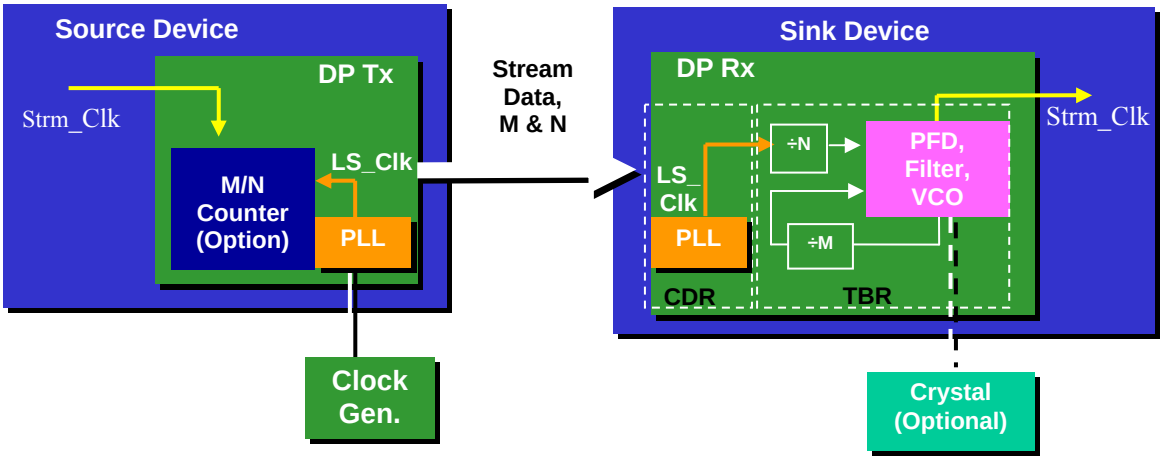



**Figure 2.17 M and N Value Determination in Asynchronous Clock Mode**

It should be noted that use of N value of 32,768 does not mandate the reference pulse period be 32,768 * t_LS_Clk which is roughly 121us for high link rate. The value of N (which is 32,768 or 8000h) and M (which is measured by the counter in the transmitter) may be divided by power of two (or right-shifted) to realize the reference pulse period suited for each implementation

Method for right-shifting M depends on the required accuracy and jitter tolerance of each application. The simplest method of rounding up to the nearest integer value (thus, resulting in approximated stream clock regeneration) may be used for certain applications where the regenerated stream timing is Gen-locked to incoming data. Other applications may use a more elaborate fractional-M PLL approach for increasing the accuracy while maintaining the low jitter.

In some implementations, in the meantime, the value of M may be accumulated multiple times to use even bigger N and M values for stream clock regeneration.,

How to use (or even not to use) M and N values for the stream clock regeneration is implementation specific.

### *2.2.3.1 De-spreading of the Regenerated Stream Clock*

The DisplayPort Specification optionally supports down-spreading of the link frequency (with modulation frequencies of 30 or 33 kHz) for minimizing EMI.

A DisplayPort Sink Device shall indicate whether it is capable of supporting down-spread link frequency in the DPCD by either setting or clearing MAX_DOWNSPREAD bit.

For a certain Sink Device, such as an audio Sink Device, the regenerated stream clock must not have down-spreading, even if its DisplayPort receiver is capable of supporting down-spread link frequency. Sink Device has two options:

- Request Source Device to disable by clearing MAX_DOWNSPREAD bit in DPCD to 0.
- Let the Source Device to down-spread by setting MAX_DOWNSPREAD bit in DPCD to 1 and perform de-spread.

Method of de-spreading is implementation specific. The following sub-section describes one of the implementation options.

#### 2.2.3.1.1 Stream Clock De-spreading Example (INFORMATIVE)

Link frequency may be spread (that is, modulated) by modulating the clock reference to DisplayPort transmitter. As far as the relationship between Link Symbol clock (LS_Clk) and Stream clock (Strm_Clk), there are two cases as follows:

- Link Symbol clock and Stream clock are equally modulated. Both clocks use the same, modulated clock reference.
- Link Symbol clock is modulated while Stream clock is not. They use different clock references.

In both case, LS_Clk count and Strm_Clk count are consistent per integer multiple of modulation period, t_mod.

The receiver uses a counter running at its local reference clock rate (clock period = t_ref) to determine t_mod. First, it sets the counter clear value to be:

- COUNTER_CLEAR_VALUE (initial) = 32 * (1/f_mod) / t_ref,

where f_mod is either 30 or 33 kHz as indicated by the transmitter in DOWNSPREAD_CTRL byte.

When COUNTER_CLEAR_VALUE * t_ref is equal to the 32 * t_mod, the LS_Clk count per that period shall be consistent over multiple measurements. The receiver uses this criterion for determining the COUNTER_CLEAR_VALUE (final).

Then the receiver measures the regenerated Strm_Clk count per the period of COUNTER_CLEAR_VALUE (final) * t_ref. This measured Strm_Clk count (Strm_Clk_Count) is used by the receiver to generate a Despread_Strm_Clk:

- t_Despread_Strm_Clk = CONTER_CLEAR_VALUE(final) * t_ref / Strm_Clk_Count

### 2.2.4 Main Stream Attribute Data Transport

This section describes Main Stream Attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes shall be as follows:

- M and N for stream clock recovery (24 bits each)
- Horizontal and Vertical Totals of the transmitted main video stream, in pixel and line counts, respectively (16 bits each)
- Horizontal and Vertical active start from the leading edges of Hsync and Vsync in pixel and line counts, respectively (16 bits each)
- Hsync polarity/Hsync width and Vsync polarity and Vsync width in pixel and line count, respectively (1 bit for polarity and 15 bits for width)
- Active video width and height in pixel and line counts, respectively (16 bits each)
- Miscellaneous (8 bits)
  - Synchronous Clock (bit 0)
    - 0 = Link clock and stream clock asynchronous
    - 1 = Link clock and stream clock synchronous
      (When 1, the value M shall be constant unless link clock down-spread enabled)
  - Component format (bits 2:1)
    - 00 = RGB
    - 01 = YCbCr422
    - 10 = YCbCr444
    - 11 = Reserved
  - Dynamic range (bit 3)
    - 0 = VESA range (from 0 to the maximum)
    - 1 = CEA range
  - YCbCr Colorimetry (bit 4)
    - 0 = ITU-R BT601-5
    - 1 = ITU-R BT709-5
  - Bit depth per color/component (bits 7:5)
    - 000 = 6 bits
    - 001 = 8 bits
    - 010 = 10 bits
    - 011 = 12 bits
    - 100 = 16 bits
    - 101, 110, 111 = Reserved

These Main Stream Attribute data shall be transported as shown in Figure 2.18 (after 2-LS_Clk inter-lane de-skewing).

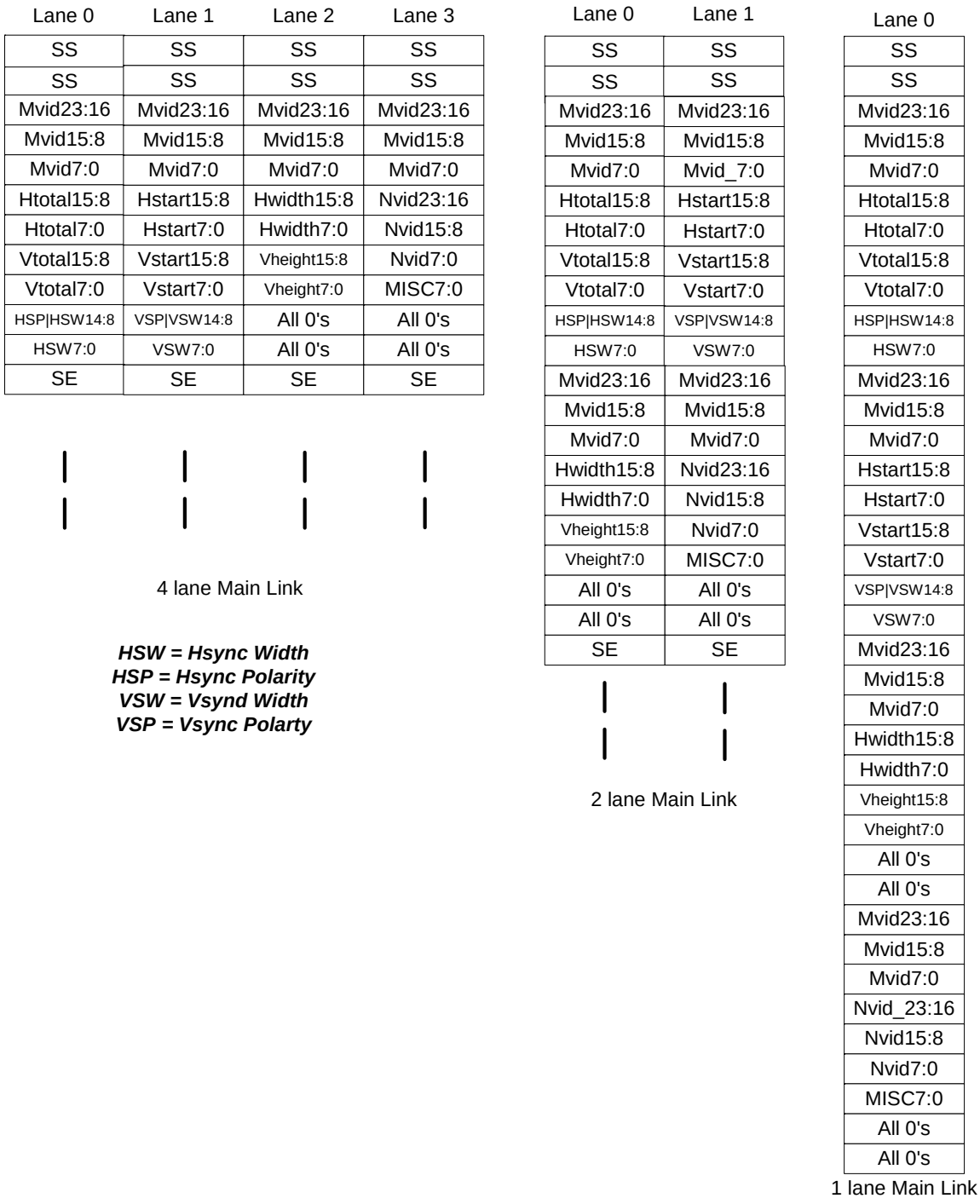



**Figure 2.18 Transport of DisplayPort_MainStream_Attribute**

The Main Stream Attributes shall be distinguished from secondary-data packet by the fact that it starts with two consecutive “SS” symbols per lane.

### 2.2.5 Secondary-data Packing Formats

Table 2.32 shows how the secondary-data packet is constructed.

**Table 2.32 Secondary-data Packet Header**

| Byte# | Content |
|---|---|
| HB0 | Secondary-data Packet ID |
| HB1 | Secondary-data Packet Type |
| HB2 | Secondary-data-packet-specific Header Byte0 |
| HB3 | Secondary-data-packet-specific Header Byte1 |

For DisplayPort Version 1.0, the following packet types are defined as shown in Table 2.33.

**Table 2.33 Secondary-data Packet Type**

| Packet Type Value | Packet Type | Transmission Timing |
|---|---|---|
| 00h | DisplayPort Reserved | |
| 01h | Audio_TimeStamp Packet | Once per video frame during V-blank, 24-byte data |
| 02h | Audio_Stream Packet | Once per video line during H/V-blank, 1024 data bytes max. |
| 03h | DPCP Synchronization Packet | Once per video frame during V-blank 32 data bytes max. |
| 04h - 7Fh | DisplayPort Reserved | |
| 80h + InfoFrame Type | EIA/CEA-861C InfoFrame Packets | Once per video frame during V-blank, 28 data bytes |

**Note 1:** Audio Stream Packet size shall be constant whether the main stream video is in vertical display period or in vertical blanking period.

**Note 2:** As for DPCP Synchronization Packet, refer to APPENDIX 1 on p.204.

If there are multiple audio streams transported simultaneously, secondary-data packet ID in HB0 shall be used to associate Audio Stream Packet to its Audio Time Stamp packet and CEA-861C Audio InfoFrame packet.

### *2.2.5.1 InfoFrame Packet*

Figure 2.19 shows InfoFrame packet over Main Link. (As for the parity bytes, or PB's in the diagram, refer to Section 2.2.6.) DisplayPort Device compliant with DisplayPort Specification Version 1.0 shall comply with EIA/CEA-861C when using InfoFrame. In other words, the usage of AVI InfoFrame Version 1.0 is prohibited.

InfoFrame packets shall be sent once per frame during the vertical blanking period of the main video stream. For the transport of Audio InfoFrame packet without main video stream, refer to Section 2.2.5.3.6 on p.74.

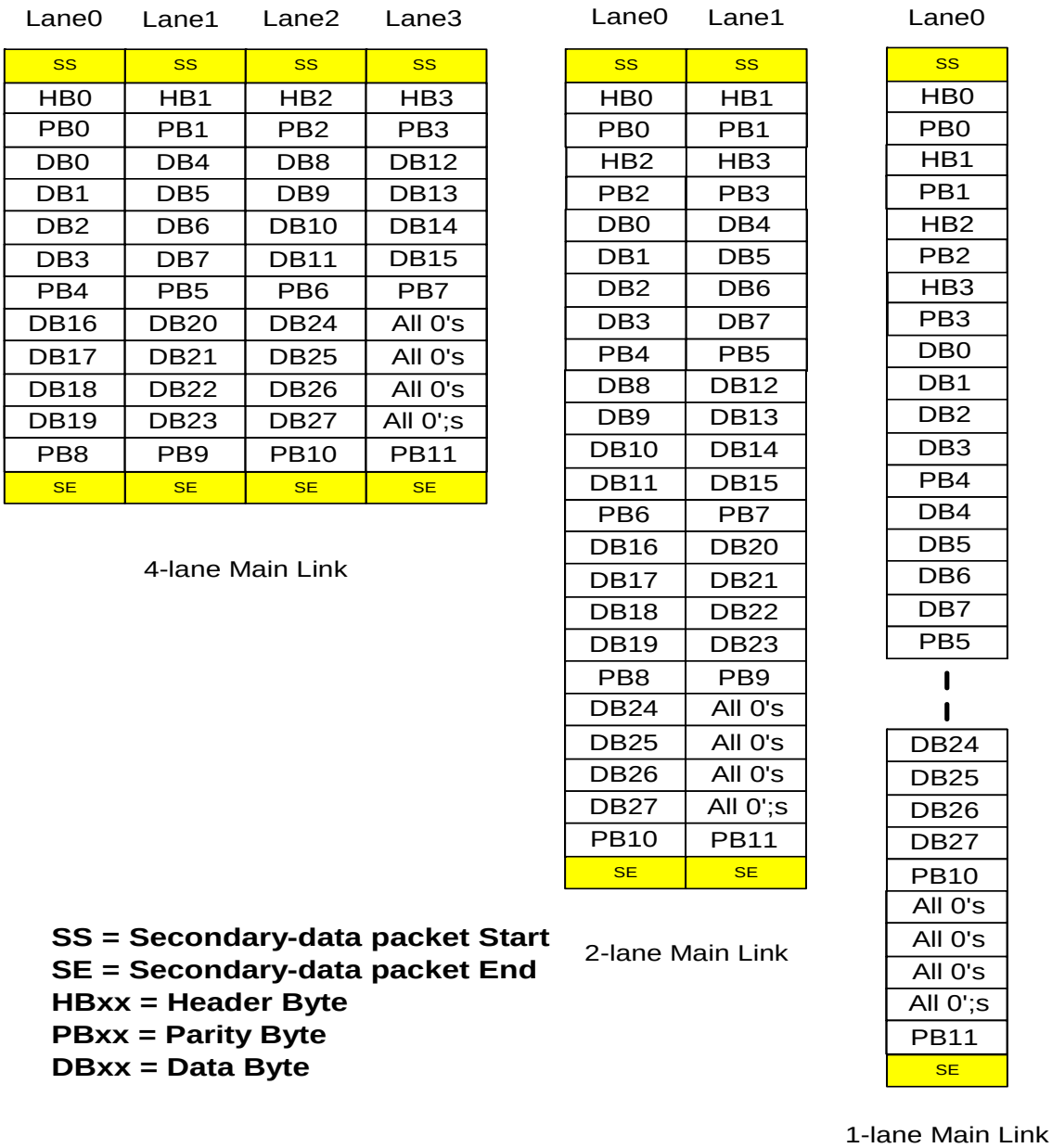



**Figure 2.19 InfoFrame Packet**

#### 2.2.5.1.1 InfoFrame Packet Header

Table 2.34 summarizes the packet header bytes of InfoFrame packets

**Table 2.34 Header Bytes of InfoFrame Packet**

| Byte# | Content |
|---|---|
| HB0 | Secondary-data Packet ID<br>InfoFrame packet, Audio Time Stamp packet, and Audio Stream packet shall have the same Packet ID when they are associated with the same audio stream. |
| HB1 | 80h + InfoFrame Type value |
| HB2 | Bits 7:0 = Least significant 8 bits of (Data Byte Count – 1)<br>For InfoFrame, the value shall be 1Bh (that is, Data Byte Count = 28 bytes. Unused bytes shall be zero-padded.) |
| HB3 | Bits 1:0 = Most significant 2 bits of (Data Byte Count – 1)<br>Bits 7:2 = DisplayPort Version Number<br>(10h, or 010000 binary for Version 1.0) |

### *2.2.5.2 Audio_TimeStamp Packet*

Figure 2.20 shows Audio_TimeStamp packet over Main Link.

The Audio_TimeStamp packet shall be sent once per frame during the vertical blanking period of the main video stream after Audio InfoFrame packet. For the transport of Audio_TimeStamp packet without main video stream, refer to Section 2.2.5.3.6 on p.74.

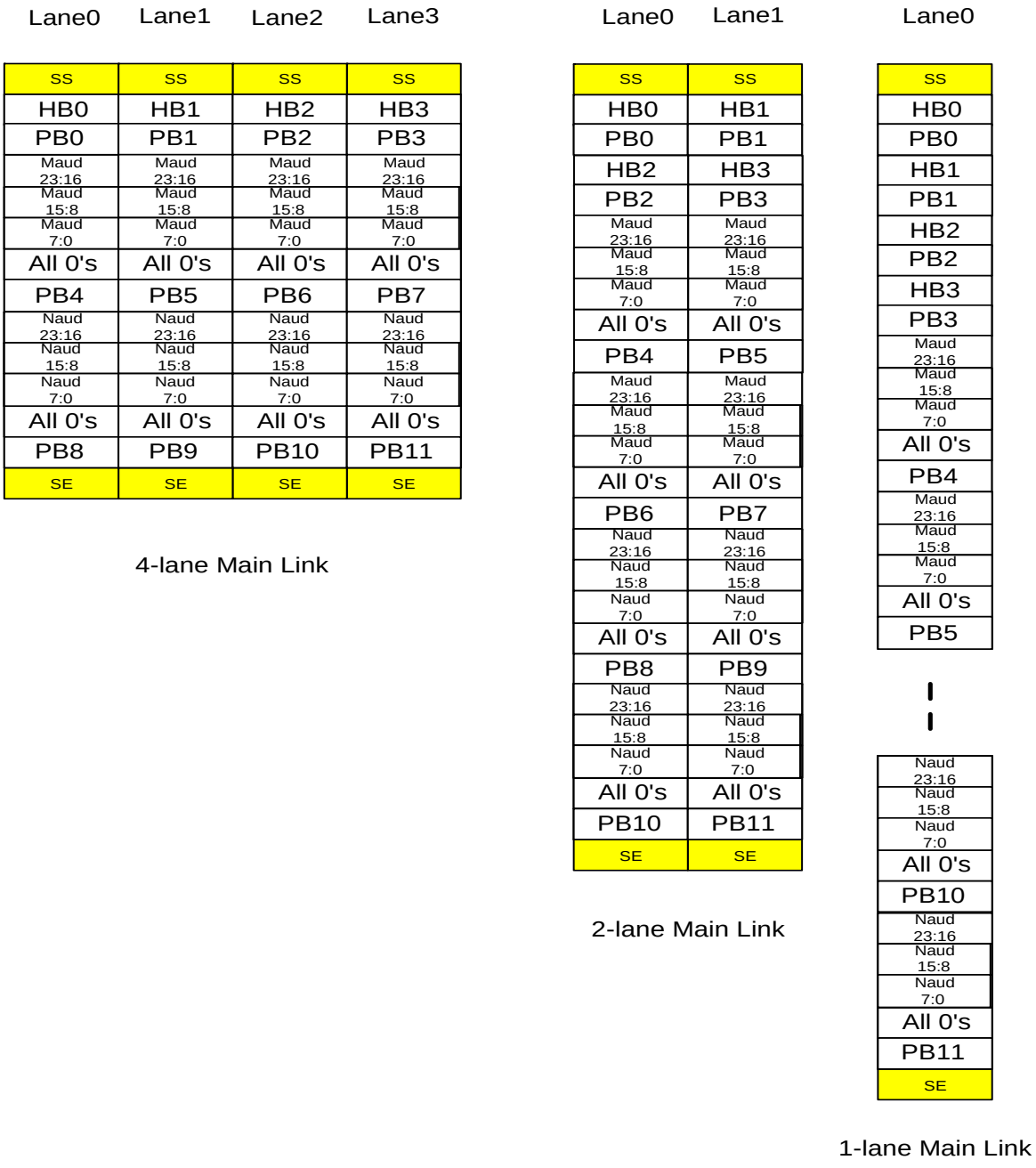



**Figure 2.20 Audio_TimeStamp Packet**

Audio_TimeStamp consists of Maud23:0 and Naud23:0. The relationship of Maud and Naud is expressed in the following equation:

- Maud/Naud = 512 * fs / f_LS_Clk

where fs is the sampling frequency of the audio stream being transported.

In addition to the Audio_TimeStamp packet, the Maud7:0 are transported once per main video stream horizontal line period immediately following Mvid7:0.

#### 2.2.5.2.1 Audio_TimeStamp Packet Header

Table 2.35 describes the packet header bytes of Audio Time Stamp packets

**Table 2.35 Header Bytes of Audio_TimeStamp Packet**

| Byte# | Content |
|---|---|
| HB0 | Secondary-data Packet ID<br>InfoFrame packet, Audio Time Stamp packet, and Audio Stream packet shall have the same Packet ID when they are associated with the same audio stream. |
| HB1 | 01h |
| HB2 | Bits 7:0 = Least significant 8 bits of (Data Byte Count – 1)<br>For Audio Time Stamp packet, the value shall be 17h (that is, Data Byte Count = 24 bytes). Unused bytes shall be zero-padded. |
| HB3 | Bits 1:0 = Most significant 2 bits of (Data Byte Count – 1)<br>Bits 7:2 = DisplayPort Version Number<br>(10h, or 010000 binary for Version 1.0) |

#### 2.2.5.2.2 Audio Time Stamp Values

Table 2.36 shows the audio time stamp values for various audio sampling frequencies when audio clock and Link Symbol clock are synchronous.

Note that either when down-spreading of the link is enabled or audio clock is asynchronous to the link symbol clock, the value of M will change over time. As is the case with Mvid measurement, the Naud shall be set to $2^{15}$ (= 32768) for Maud measurement in asynchronous clock mode.

**Table 2.36 Examples of Maud and Naud Values**

| f_LS_Clk=270MHz (2.7Gbps) | | f_LS_Clk=162MHz (1.62Gbps) | |
|---|---|---|---|
| Regenerated clock = 512x 48kHz<br>(Used when fs = integer multiple of 48kHz) | | | |
| Maud = | 512 | M = | 512 |
| Naud = | 5625 | N = | 3375 |
| Regenerated clock = 512x 44.1kHz<br>(Used when fs = integer multiple of 44.1kHz) | | | |
| Maud = | 784 | M = | 784 |
| Naud = | 9375 | N = | 5625 |
| Regenerated clock = 512x 32kHz<br>(Used when fs = integer multiple of 32kHz, but not integer multiple of 48kHz) | | | |
| Maud = | 1024 | M = | 1024 |
| Naud = | 16875 | N = | 10125 |

**Note**: No down-spreading, with synchronous clock, assumed.

### *2.2.5.3 Audio_Stream Packet*

Transport of audio stream is an optional. When audio stream is transported, the AudioInfoFrame packet describing the attribute of the audio stream and Audio Timestamp packet shall be also transported, each once per frame during the vertical blanking period of the main video stream.

Audio_Stream packets shall be sent during both horizontal and vertical blanking period of the main video stream. In order to minimize the buffer size requirement, the Audio_Stream packet size shall be constant both during vertical display period and vertical blanking period.

#### 2.2.5.3.1 Audio_Stream Packet Header

Table 2.37 describes the packet header of Audio_Stream packet.

**Table 2.37 Header Bytes of Audio_Stream Packet**

| Byte# | Content |
|---|---|
| HB0 | Secondary-data Packet ID<br>InfoFrame packet, Audio Time Stamp packet, and Audio Stream packet shall have the same Packet ID when they are associated with the same audio stream. |
| HB1 | 02h |
| HB2 | Reserved (all 0's) |
| HB3 | Bits 2:0 = ChannelCount<br>Actual channel count – 1<br>Bit 3 = Reserved (= 0)<br>Bits 7:4 = Coding Type<br>0000 = IEC60958-like coding<br>All other values are reserved for DisplayPort Ver.1.0 |

#### 2.2.5.3.2 Audio_Stream Data Mapping Over Main Link

Channel count is the count of audio channels transmitted through DisplayPort link. Receiver shall use this 3-bit value to decide how to interpret the payload of Audio Stream Packet. One to eight channels are supported in DisplayPort Ver.1.0.

Figure 2.21 shows the Audio_Stream Packet mapping over Main Link for 1 - 2 channel audio while Figure 2.22 shows the mapping for 3 - 8 channel mapping.

The 1 and 2 channel audio share the same Audio_Stream packet structure as shown in Figure 2.21 . So do the 3 - 8 channel audio as shown in Figure 2.22 . Which channels to map the audio data depends on audio-data-to-speaker mapping, as described in Section 2.2.5.3.3. Unused channels shall be marked with the SP bit (sample present) bit cleared to 0 in the packet payload, as described in Section 2.2.5.3.4.

Audio_Stream packet transfer shall not stop in the middle of an audio sample. For example, when a 2-channel audio is transmitted over 1 lane Main Link, the packet may be ended after PB5 in Figure 2.21 since the transmission of Sample 0 is completed at that point. However, it shall not end after PB4.

| 4 lane Main Link | | | |
|---|---|---|---|
| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
| SS | SS | SS | SS |
| HB0 | HB1 | HB2 | HB3 |
| PB0 | PB1 | PB2 | PB3 |
| S0 Ch0 B0 | S0 Ch1 B0 | S1 Ch0 B0 | S1 Ch1 B0 |
| S0 Ch0 B1 | S0 Ch1 B1 | S1 Ch0 B1 | S1 Ch1 B1 |
| S0 Ch0 B2 | S0 Ch1 B2 | S1 Ch0 B2 | S1 Ch1 B2 |
| S0 Ch0 B3 | S0 Ch1 B3 | S1 Ch0 B3 | S1 Ch1 B3 |
| PB4 | PB5 | PB6 | PB7 |
| S2 Ch0 B0 | S2 Ch1 B0 | S3 Ch0 B0 | S3 Ch1 B0 |
| S2 Ch0 B1 | S2 Ch1 B1 | S3 Ch0 B1 | S3 Ch1 B1 |
| S2 Ch0 B2 | S2 Ch1 B2 | S3 Ch0 B2 | S3 Ch1 B2 |
| S2 Ch0 B3 | S2 Ch1 B3 | S3 Ch0 B3 | S3 Ch1 B3 |
| PB8 | PB9 | PB10 | PB11 |

"S" stands for Sample, "B" for Byte, and "Ch" for Channel. For example, S0_Ch0_B0 means the Byte 0 of Channel 0 of Sample 0.

| 2 lane Main Link | |
|---|---|
| Lane 0 | Lane 1 |
| SS | SS |
| HB0 | HB1 |
| PB0 | PB1 |
| HB1 | HB2 |
| PB2 | PB3 |
| S0 Ch0 B0 | S0 Ch1 B0 |
| S0 Ch0 B1 | S0 Ch1 B1 |
| S0 Ch0 B2 | S0 Ch1 B2 |
| S0 Ch0 B3 | S0 Ch1 B3 |
| PB4 | PB5 |
| S1 Ch0 B0 | S1 Ch1 B0 |
| S1 Ch0 B1 | S1 Ch1 B1 |
| S1 Ch0 B2 | S1 Ch1 B2 |
| S1 Ch0 B3 | S1 Ch1 B3 |
| PB7 | PB8 |
| S2 Ch0 B0 | S2 Ch1 B0 |
| S2 Ch0 B1 | S2 Ch1 B1 |
| S2 Ch0 B2 | S2 Ch1 B2 |
| S2 Ch0 B3 | S2 Ch1 B3 |

| 1 lane Main |
|---|
| Lane 0 |
| SS |
| HB0 |
| PB0 |
| HB1 |
| PB1 |
| HB2 |
| PB2 |
| HB3 |
| PB3 |
| S0 Ch0 B0 |
| S0 Ch0 B1 |
| S0 Ch0 B2 |
| S0 Ch0 B3 |
| PB4 |
| S0 Ch1 B0 |
| S0 Ch1 B1 |
| S0 Ch1 B2 |
| S0 Ch1 B3 |
| PB5 |

**Figure 2.21 Audio_Stream Packet over Main Link for 1 - 2 ch Audio**

4 lane Main Link

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| SS | SS | SS | SS |
| HB0 | HB1 | HB2 | HB3 |
| PB0 | PB1 | PB2 | PB3 |
| S0 Ch0 B0 | S0 Ch1 B0 | S0 Ch2 B0 | S0 Ch3 B0 |
| S0 Ch0 B1 | S0 Ch1 B1 | S0 Ch2 B1 | S0 Ch3 B1 |
| S0 Ch0 B2 | S0 Ch1 B2 | S0 Ch2 B2 | S0 Ch3 B2 |
| S0 Ch0 B3 | S0 Ch1 B3 | S0 Ch2 B3 | S0 Ch3 B3 |
| PB4 | PB5 | PB6 | PB7 |
| S0 Ch4 B0 | S0 Ch5 B0 | S0 Ch6 B0 | S0 Ch7 B0 |
| S0 Ch4 B1 | S0 Ch5 B1 | S0 Ch6 B1 | S0 Ch7 B1 |
| S0 Ch4 B2 | S0 Ch5 B2 | S0 Ch6 B2 | S0 Ch7 B2 |
| S0 Ch4 B3 | S0 Ch5 B3 | S0 Ch6 B3 | S0 Ch7 B3 |
| PB8 | PB9 | PB10 | PB11 |
| S1 Ch0 B0 | S1 Ch1 B0 | S1 Ch2 B0 | S1 Ch3 B0 |
| S1 Ch0 B1 | S1 Ch1 B1 | S1 Ch2 B1 | S1 Ch3 B1 |
| S1 Ch0 B2 | S1 Ch1 B2 | S1 Ch2 B2 | S1 Ch3 B2 |
| S1 Ch0 B3 | S1 Ch1 B3 | S1 Ch2 B3 | S1 Ch3 B3 |
| PB12 | PB13 | PB14 | PB15 |

"S" stands for Sample, "B" for Byte, and "Ch" for Channel. For example, S0_Ch0_B0 means the Byte 0 of Channel 0 of Sample 0.

2 lane Main Link

| Lane 0 | Lane 1 |
|---|---|
| SS | SS |
| HB0 | HB1 |
| PB0 | PB1 |
| HB2 | HB3 |
| PB2 | PB3 |
| S0 Ch0 B0 | S0 Ch1 B0 |
| S0 Ch0 B1 | S0 Ch1 B1 |
| S0 Ch0 B2 | S0 Ch1 B2 |
| S0 Ch0 B3 | S0 Ch1 B3 |
| PB4 | PB5 |
| S0 Ch2 B0 | S0 Ch2 B0 |
| S0 Ch2 B1 | S0 Ch2 B1 |
| S0 Ch2 B2 | S0 Ch2 B2 |
| S0 Ch2 B3 | S0 Ch2 B3 |
| PB6 | PB7 |
| S0 Ch4 B0 | S0 Ch5 B0 |
| S0 Ch4 B1 | S0 Ch5 B1 |
| S0 Ch4 B2 | S0 Ch5 B2 |
| S0 Ch4 B3 | S0 Ch5 B3 |
| PB8 | PB9 |
| S0 Ch6 B0 | S0 Ch7 B0 |
| S0 Ch6 B1 | S0 Ch7 B1 |
| S0 Ch6 B2 | S0 Ch7 B2 |
| S0 Ch6 B3 | S0 Ch7 B3 |
| PB10 | PB11 |
| S1 Ch0 B0 | S1 Ch1 B0 |
| S1 Ch0 B1 | S1 Ch1 B1 |
| S1 Ch0 B2 | S1 Ch1 B2 |
| S1 Ch0 B3 | S1 Ch1 B3 |
| PB12 | PB13 |

1 lane Main

| Lane 0 |
|---|
| SS |
| HB0 |
| PB0 |
| HB1 |
| PB1 |
| HB2 |
| PB2 |
| HB3 |
| PB3 |
| S0 Ch0 B0 |
| S0 Ch0 B1 |
| S0 Ch0 B2 |
| S0 Ch0 B3 |
| PB4 |
| S0 Ch1 B0 |
| S0 Ch1 B1 |
| S0 Ch1 B2 |
| S0 Ch1 B3 |
| PB5 |
| S0 Ch2 B0 |
| S0 Ch2 B1 |
| S0 Ch2 B2 |
| S0 Ch2 B3 |
| PB6 |
| S0 Ch3 B0 |
| S0 Ch3 B1 |
| S0 Ch3 B2 |
| S0 Ch3 B3 |
| PB7 |
| S0 Ch4 B0 |
| S0 Ch4 B1 |
| S0 Ch4 B2 |
| S0 Ch4 B3 |
| PB8 |
| S0 Ch5 B0 |
| S0 Ch5 B1 |
| S0 Ch5 B2 |
| S0 Ch5 B3 |
| PB9 |
| S0 Ch6 B0 |
| S0 Ch6 B1 |
| S0 Ch6 B2 |
| S0 Ch6 B3 |
| PB10 |

**Figure 2.22 Audio Stream Packet over Main Link for 3 - 8 ch Audio**

#### 2.2.5.3.3 Speakers mapping

Transported audio channel data shall be mapped to speakers according to 8-bit data, CA7:0, which is transported as Data Byte 4 within Audio InfoFrame, as defined in Section 6.6.2 of CEA-861-C document.

#### 2.2.5.3.4 Data Mapping within Audio_Stream Packet Payload

Audio_Stream packet payload consists of 4 bytes of data per lane, each 4 bytes protected by a parity byte.

Figure 2.23 shows the data mapping within the 4-byte payload of Audio_Stream packet with IEC60958-like coding type. In the previous two figures (Figure 2.21and Figure 2.22), these 4 bytes correspond to, for example, S0_Ch0_B0, S0_Ch0_B1, S0_Ch0_B2, and S0_Ch0_B3.

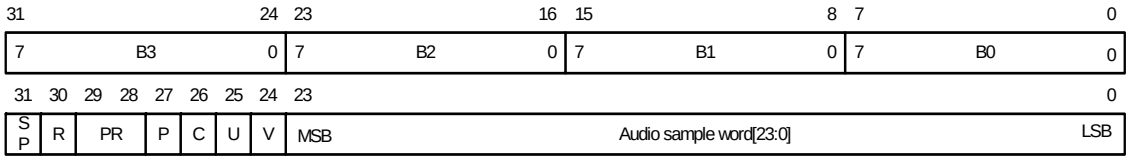



**Figure 2.23 Data Mapping Within 4-Byte Payload of Audio_Stream Packet**

Table 2.38 shows the bit definition of the 4-byte payload shown in Figure 2.23.

**Table 2.38 Bit Definition of Payload of Audio_Stream Packet with IEC60958-like Coding**

| Bit name | Bit position | Description |
|---|---|---|
| Audio sample word | Byte 2 bits 7:0<br>Byte 1 bits 7:0<br>Byte 0 bits 7:0 | Audio data. Content of this data depends from the audio coding type. In case of L-PCM audio most significant bit of the audio is placed at the Byte 2 bit 7 position. If audio data size is less than 24-bits then unused least significant bits shall be zero-padded. |
| V | Byte 3 bit 0 | Validity flag |
| U | Byte 3 bit 1 | User bit |
| C | Byte 3 bit 2 | Channel status |
| P | Byte 3 bit 3 | Parity bit |
| PR | Byte 3 bits 5:4 | Preamble code and its correspondence with IEC-60958 preamble :<br>00 – Subframe 1 and start of the audio block (11101000 preamble)<br>01 – Subframe 1 (1110010 preamble)<br>10 – Subframe 2 (1110100 preamble) |
| R | Byte 3 bit 6 | Reserved bit. It should be 0. |
| SP | Byte 3 bit 7 | Sample present bit:<br>1 – Sample information is present and can be processed.<br>0 – Sample information is not present.<br><br>All channels of one sample must have the same value of the sample present bit.<br><br>This bit is especially useful when 2-ch audio is transported over 4-lane Main Link. In this operation, Main Link lanes 2 and 3 may or may not have the audio sample data. This bit indicates whether the audio sample is present or not. |

#### 2.2.5.3.5 Other Audio Formats (INFORMATIVE)

DisplayPort Specification Ver.1.0, only IEC60958-like packing format type is supported. Using this format type, 1 - 8 ch LPCM, AC3, and DTS audio stream can be transported. Other audio packing formats may be added in the future revision of DisplayPort specification while maintaining the consistent secondary-data mapping specification described in this document.

#### 2.2.5.3.6 Transport of Audio Packets Without Main Video Stream

DisplayPort Specification Ver.1.0 supports the transport of audio stream while no video stream is being transported over the link.

When the link is active without main video stream, Source Device shall insert BS symbol followed by VB-ID, Mvid7:0, and Maud7:0, referred to as "BS symbol set", every $2^{13}$, or 8,192 link symbols. Both NoVideoStream_Flag and VerticalBlanking_Flag of VB-ID shall be set to 1 in this condition and Mvid7:0 is set to 00h. Source Device shall transmit Audio_Stream packet after each BS symbol set. Furthermore, Source Device shall insert Audio InfoFrame packet and Audio_TimeStamp packet once after every $512^{th}$ BS symbol set.

### 2.2.6 ECC for Secondary-data Packet

All of the secondary-data packets shall be protected via ECC. (DisplayPort Main Link Attributes data is protected via redundancy.)

The secondary-data packet shall consist of 4-byte header protected by 4-byte parity, followed by 16-byte payload data protected by 4-byte parity. The secondary-data packet shall end with parity byte. Packets constructed with fewer than 16 bytes of data shall use zero padding to fill remaining data positions.

#### *2.2.6.1 ECC Based on RS (15,13)*

DisplayPort uses Reed-Solomon code, RS(15,13), with symbol size of nibble (4 bits) in the ECC block.

The basic principle of error-correcting encoding is to find the remainder of the message divided by a generator polynomial G(x).

The encoder works by simulating a Linear Feedback Shift Register with degree equal to G(x), and feedback taps with the coefficients of the generating polynomial of the code. In general the generator polynomial G(x) for any number of parity, configurable as the NPAR is as following:

$$G(x) = (x - a^1)(x - a^2)(x - a^3)(x - a^4) \ldots (x - a^{NPAR})$$

Since RS(15,13) with symbol size of nibble is chosen, the second degree generator polynomial is used as following:

$$G(x) = (x - a^1)(x - a^2)$$
$$= x^2 - g1*x + g0$$

Note that subtraction is equivalent to addition in binary fields.

Therefore:

$$G(x) = x^2 + g1*x + g0, \quad \text{where } g1 = a^5 \text{ and } g0 = a^3$$

With encoding of the base field GF(2^4), "a" is equal to (0, 0, 1, 0) which gives a^5 = (0, 1, 1, 0) and a^3 = (1, 0, 0, 0).

The logic equations for implementing g1 and g0 multiplications are listed below:

g1*c[3:0] = {c[2]^c[1], c[3]^c[1]^c[0], c[2]^c[0], c[3]^c[2]}

g0*c[3:0] = {c[3]^c[0], c[3]^c[2], c[2]^c[1], c[1]}

//==========

The following three messages show the outputs of ECC for input data with parity nibbles shown in underlined, bold, italic-font numbers.

---------- Transmitted Message ----------

f, e, d, c, b, a, 9, 8, ***e, 9,***

---------- Transmitted Message ----------

9, 8, 3, 2, 1, 7, 5, 4, ***f, 1,***

---------- Transmitted Message ----------

7, 6, 5, 9, 8, 1, 3, 2, ***7, 2,***

==========

### *2.2.6.2 ECC g1 and g0 C-Code (INFORMATIVE)*

Figure 2.24 shows the block diagram of RS (15,13) encoder with symbol size of nibble.

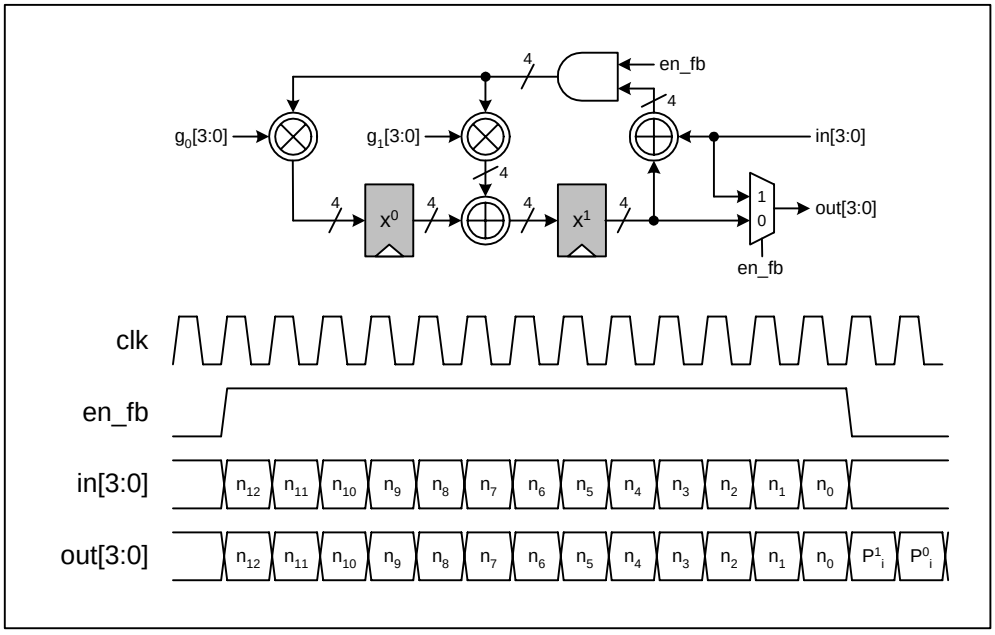



**Figure 2.24 Block Diagram of RS(15:13) Encoder**

The code below shows ECC g1 and g0 in C code.

```
//-----------------------------------------------------
//   c * a^3
//-----------------------------------------------------
unsigned char gfmul_3( unsigned char ) ;
unsigned char gfmul_3( a )
unsigned char a ;
{
int i ;
unsigned char c[8], gf_mul[8], r ;

  for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply */
    c[i] = a & 0x01 ;
    a = a >> 1 ;
  }

gf_mul[0] = c[1] ;
gf_mul[1] = c[1] ^ c[2] ;
gf_mul[2] = c[2] ^ c[3] ;
gf_mul[3] = c[0] ^ c[3] ;
r = 0 ;
for ( i=0; i<4; i++) {
  r = ((gf_mul[i] & 0x01) << i) | r ;
}

return (r) ;
}

//-----------------------------------------------------
//  c * a^5
//-----------------------------------------------------
unsigned char gfmul_5( unsigned char ) ;
unsigned char gfmul_5( a )
unsigned char a ;
```

```
{
int i ;
unsigned char c[8], gf_mul[8], r ;

  for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply */
    c[i] = a & 0x01 ;
    a = a >> 1 ;
  }

gf_mul[0] = c[2] ^ c[3] ;
gf_mul[1] = c[0] ^ c[2] ;
gf_mul[2] = c[0] ^ c[1] ^ c[3] ;
gf_mul[3] = c[1] ^ c[2] ;
r = 0 ;
for ( i=0; i<4; i++) {
  r = ((gf_mul[i] & 0x01) << i) | r ;
}

return (r) ;
}
//-------------------------------------------------------
```

### *2.2.6.3 Nibble Interleaving*

To further enhance the error correcting capability, ECC block of DisplayPort incorporates nibble-interleaving after the incoming data packet is error-correcting encoded. Combining RS(15:13) with the nibble-interleaving, the ECC block is capable of correcting up to 2-byte error in a 16-byte data block.

As shown in Figure 2.25 Lane 0 is interleaved with Lane 1, while Lane 2 is interleaved with Lane 3 for 2 and 4 lane Main Link configurations. Interleaving for 1 lane Main Link is shown in Figure 2.26.

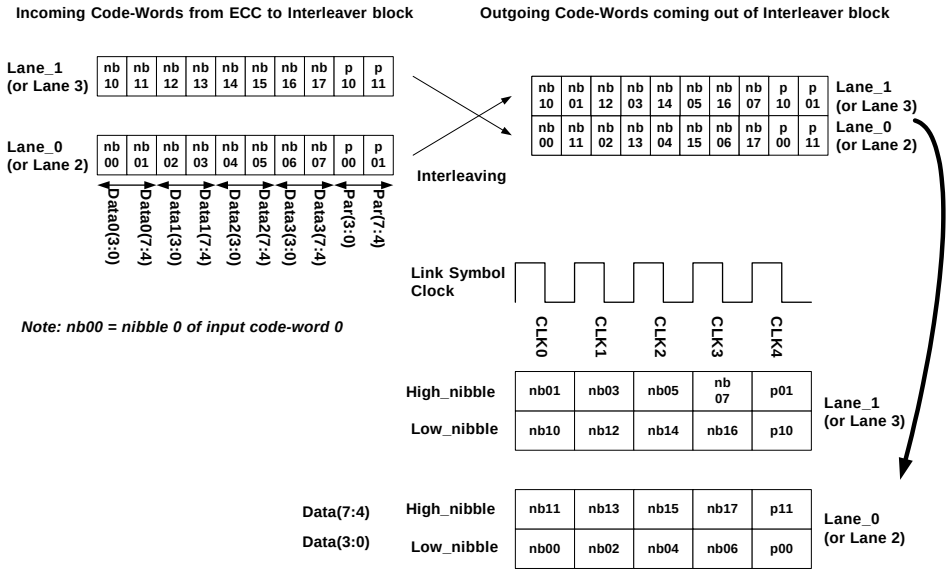



**Figure 2.25 Nibble-Interleaving in the ECC Block for 2 and 4 lane Main Link**

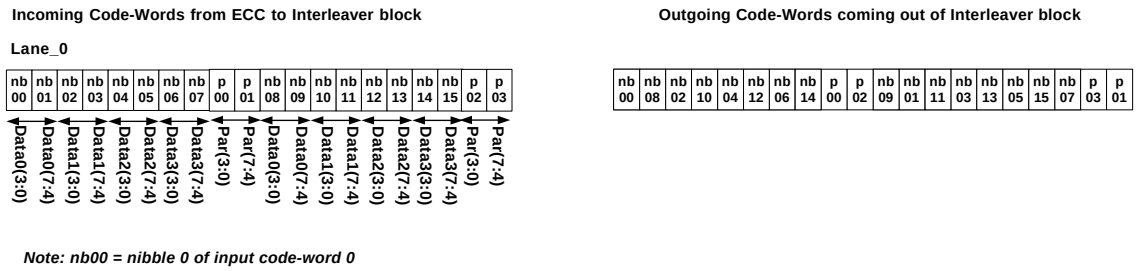



**Figure 2.26 Nibble-Interleaving in the ECC Block for 1 lane Main Link**

Since the symbol size is a nibble (4 bits wide), the length of the code word is 15 nibbles (= $2^4 - 1$) within the ECC block.

For packet payload, 2 parity nibbles (or 1 byte) shall be generated for 8 data nibbles (or 4 bytes) for the packet payload per lane as shown in Figure 2.27. Only10 nibbles consisting of 8 data nibbles and 2 parity nibbles shall be used. The remaining most significant 5 nibbles shall be zero-padded, and shall not be transmitted over DisplayPort link.

As for the packet header, 4 nibbles of the 15 nibbles shall be used as shown in Figure 2.28. Those 4 nibbles consist of 2 data (that is, packet header) nibbles and 2 parity nibbles. The remaining most

significant 11 nibbles shall be zero-padded, and shall not be transmitted. With this protection, the ECC block is capable of correcting 2-byte error in a 4-byte packet header.

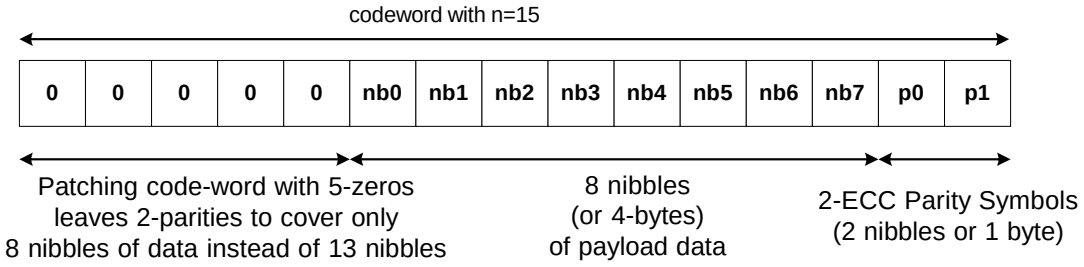



**Figure 2.27 Make-up of 15-nibble code word for Packet Payload**

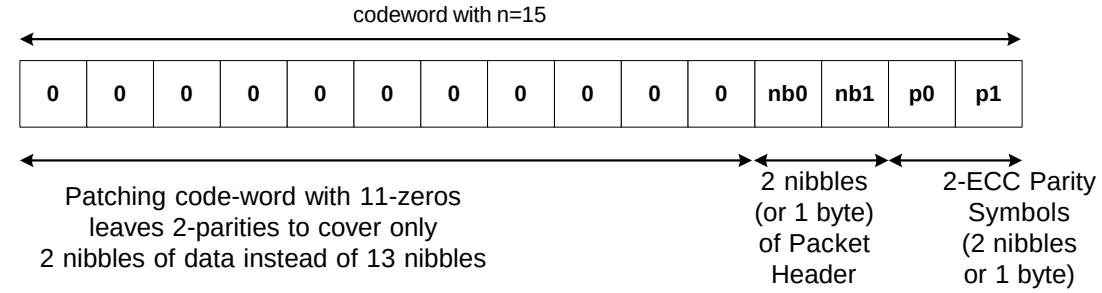



**Figure 2.28 Make-up of 15-nibble code word for Packet Header**

## *2.3 AUX CH States and Arbitration*

### 2.3.1 AUX CH STATES Overview

AUX CH of DisplayPort is a half-duplex, bi-directional channel. Source Device is the master of AUX CH (called AUX CH Requester) while the Sink is the slave (AUX CH Replier). As the master, the Source Device shall initiate a Request Transaction, to which the Sink responds with Reply Transaction.

Upon detecting Sink through Hot Plug-Detect mechanism as described in Chapter 3 of DisplayPort Specification, the Source Device shall put its AUX CH to AUX IDLE State, S2 (Figure 2.29). The Sink shall also be in AUX IDLE State, D1 (Figure 2.30) when it asserts the HPD signal.

Optionally, the Sink may monitor the presence of the Source Device by measuring the DP_PWR voltage. If it is monitoring the presence of Source Device, Sink Device may enter AUX IDLE state only when the Source is detected.

In state S2, the Source shall be in "Talk Mode" and shall issue a Request command as needed. The Sink, in state D1, shall be in "Listen Mode" and shall be waiting for a Request command.

Upon issuing a Request transaction, the Source shall transition to state S3, AUX Request CMD Pending State. In S3 state, the Source shall be in "Listen Mode" in which it waits for the Sink to reply. Upon receipt of Request transaction, the Sink shall go to state D2, AUX Reply CMD Pending state. Once in D2 state, the Sink shall be in "Talk Mode", ready to send reply over AUX CH.

Upon the reception of Request transaction, the Sink shall have a maximum of 200 μs (Response Timer time-out period) to reply. If, for some reason, it is not able to send the reply in 200us, the Sink shall back to D1 without reply. The Source shall wait for up to 400us (Reply Timer time-out period) upon entering S3. When no reply is received in 400us, the Source shall go back to S2 and shall be allowed to initiate Request transaction as needed.

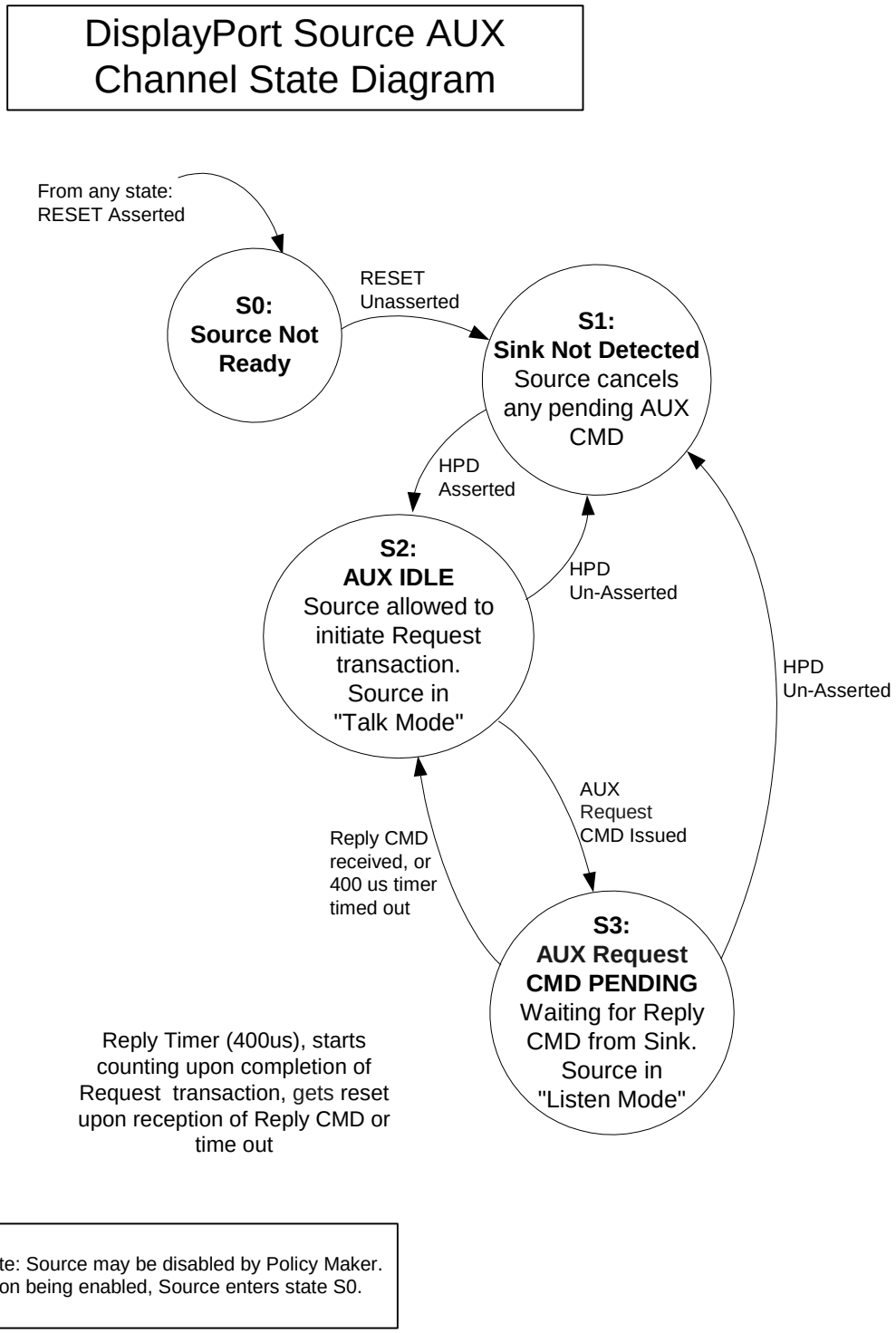



**Figure 2.29 AUX CH Source State Diagram**

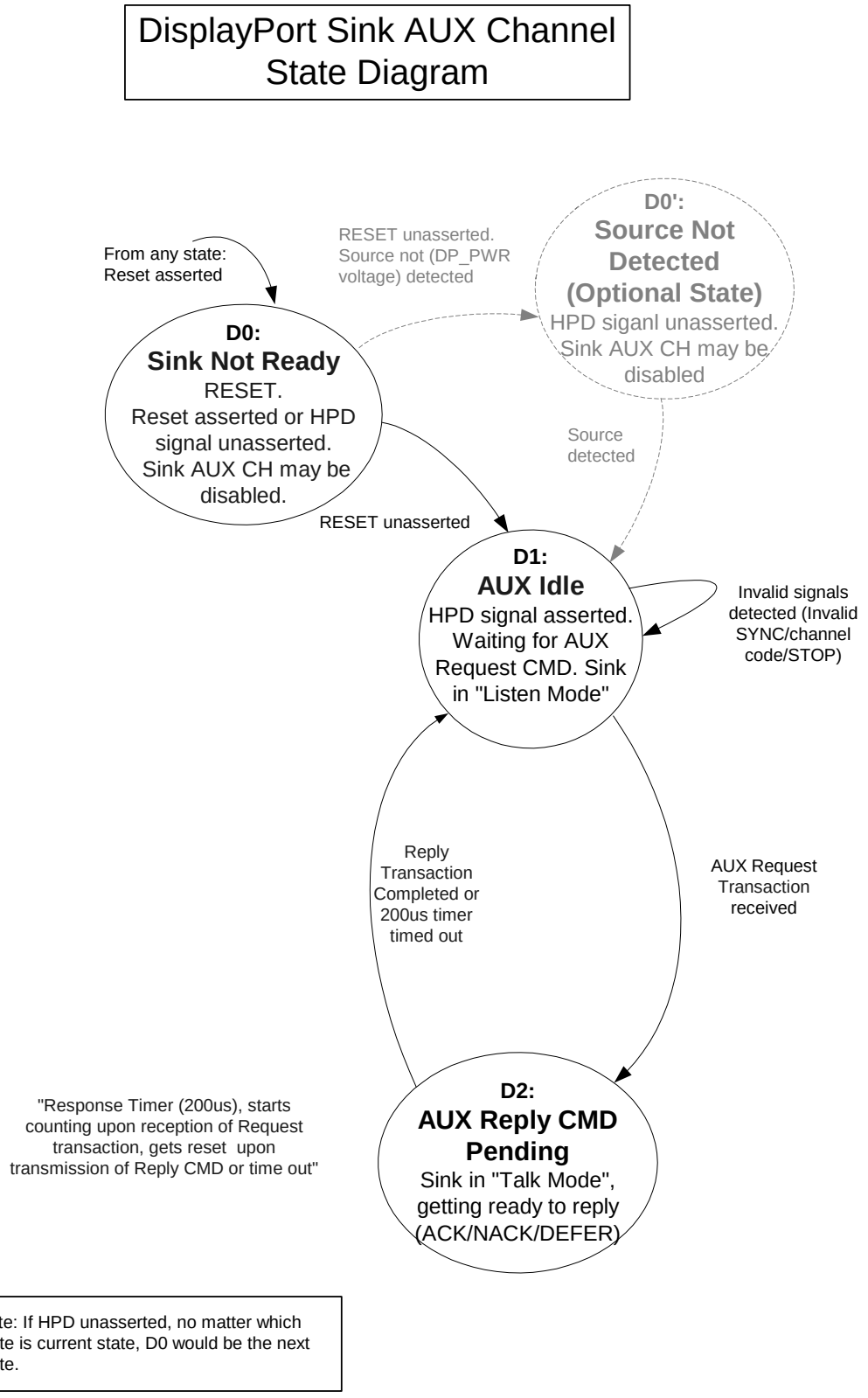



**Figure 2.30 AUX CH Sink State Diagram**

Transitions from D0 to D1 through the D0' state is used by Sink Devices that implement optional Source Device detect functionality. D0' is condition where reset is unasserted HPD signal is asserted while no Source Device is detected.

### 2.3.2 Link Layer Arbitration Control

As described above, Source and Sink shall not to be in the Talk Mode or Listen Mode at the same time. Furthermore, Response Timer time-out period of the Sink Device shall be shorter than that of Reply Timer of the Source Device. In case of time out, both the Source and Sink shall return to the AUX IDLE state, which is Talk Mode for the Source and Listen Mode for the Sink. Therefore, contention and live lock shall both be avoided.

### 2.3.3 Policy Maker AUX CH Management

There are multiple applications and services that initiate AUX CH transactions. Some of the examples are:

- AUX Link Services
  - Link capability read
  - Link configuration (training)
  - Link status read
- AUX Device Services
  - EDID read
  - MCCS (Monitor Control Command Signaling) control,

The DisplayPort AUX CH shall not support nested transactions. In other words, one transaction shall be ended before another transaction can be initiated. The Policy Maker shall be responsible for determining the order in which the multiple AUX Request transactions get executed per their priorities. Link Layer shall merely initiate AUX CH transaction as it receives the request from the Policy Maker.

A request transaction may not end in full-completion. The Sink may reply with NACK or DEFER when not ready for full-completion. The Policy Maker shall decide on the follow-up action if the Request transaction is replied with NACK or DEFER.

The amount of data transported over AUX CH per transaction shall be limited to 16 bytes or fewer at a time (that is, the burst size shall be 16 data bytes maximum). This limitation is set to prevent a single transaction from monopolizing the bus for an extended period of time. With the data rate of 1Mbps, no transaction shall occupy the AUX CH more than 500us. If a given transaction requires more than 16 bytes of data to be transported, Policy Maker shall divide it into multiple transactions with no transaction larger than 16 bytes.

### 2.3.4 Detailed Source AUX CH State Description

**State S0: Reset.** State S0 shall be entered from any state when RESET is asserted.

**State S1: AUX CH Unplugged.** The HPD signal is un-asserted (Low state). Upon entry, the level of the HPD signal shall be passed up to the Link Policy Maker. The Sink Device is either not connected or has not asserted the HPD signal. The AUX CH is unavailable. Therefore, AUX CH services such as DPCD, EDID, etc. are not available.

**State S2: Aux IDLE**. The HPD signal is asserted (High). The Sink is connected to its main power supply, though the state of the Sink Device's power switch (if any) is not specified. A message indicating AUX channel available shall be passed up to the Policy Maker. In this state no Aux Command is pending and the Aux channel is available for the Policy Maker to initiate request transactions. Source shall stay in Talk Mode until a request transaction has been completed according to AUX CH syntax as it is specified in this chapter. Upon sending STOP, the last part of request transaction, the Source shall transition to state S3 provided HPD is still asserted.

**State S3: AUX Request CMD PENDING.** Upon completion of an AUX_CH Request Transaction, the Source Aux Channel shall enter state S3. In this state, the Source shall be waiting to receive a Reply message from the Sink. The Source shall not issue commands in this state. The Source Aux Channel shall stay in Listen Mode. Upon entry to this state, Reply-Wait Timer (400 μs) shall reset and start counting. The Source AUX CH shall exit from this state and enter State S2, AUX IDLE state, when it receives the Reply Command from the Sink, or when its Reply Command Timer times out.

**Transition from any State to S0.** Occurs whenever Reset is asserted

**Transition S0:S1.** Occurs when Reset is unasserted.

**Transition S1:S2.** Occurs upon Hot Plug Detection

**Transition S2:S1 or S3:S1.** Occurs upon Hot Unplug Detection

**Transition S2:S3.** Occurs upon the completion of Source AUX CH Request Transaction

**Transition of S3:S2.** Shall take place either when Source Aux CH receives Reply Command from Sink, or when the Reply Command Timer (400 μs) times out.

### 2.3.5 Detailed Sink AUX CH State Description

**State D0: Sink Not Ready.** In this state Reset is asserted. Sink shall transition to this state from any other state when RESET is asserted. In this state, HPD signal is unasserted. Sink AUX CH may be disabled. Upon unassertion of RESET, the Sink Device shall transition to the D1 state, unless Source Device detection is implemented in which case Sink Device shall transition to the D0' state.

**State D0': Source Not Detected.** This state is optional and can be used by Sink Devices that monitors the presence of the Source. When RESET is unasserted and HPD signal is asserted and the Source is not detected, this optional state may be entered. Upon the Source Device detect, the Sink Device shall transition to D1.

**State D1: Aux Idle.** In this state Sink Aux Channel shall stay in "Listen Mode", waiting for Source to send an Aux Request Command over the AUX CH. Sink AUX CH shall also stay in this state when an invalid signal (e.g., invalid SYNC, STOP or channel code) is received. Upon receiving Aux request transaction command from Source, Sink Aux CH shall transition to state D2 and its response timer (200 μs) resets and begins counting. Note that Sink is expected to send either ACK, NACK, or DEFER reply in response to the requested transaction

**State D2: Aux Reply CMD Pending.** In this state Sink shall be in "Talk Mode", getting ready to reply to Source. Upon completion of reply transaction, Sink shall transition to D1. A time-out condition of the response timer shall cause the Sink to transition to state D1 without initiating a reply transaction.

**Transition of D0: D0' (Optional transition)** Occurs when the Reset is unasserted and HPD signal is asserted.

**Transition of D0':D1 (Optional transition)** Occurs upon Source detect after the optional state of D0' is entered

**Transition of D0:D1.** Occurs when RESET is unasserted and when the Sink Device has asserted HPD signal and is ready to serve for AUX CH services

**Transition of D1:D2.** Occurs upon receiving AUX Request transaction from Source

**Transition of D2:D1.** Occurs when the Sink completes its reply to the Source, or the Sink fails to reply before response timer (200 μs) times out

## 2.4 AUX CH Syntax

Syntaxes used for various AUX CH services are described in this section.

The following two categories are explained:

- Native AUX CH Syntax
- Mapping of $I^2C$ onto AUX CH Syntax

This section describes the DisplayPort AUX CH transaction syntax suitable for a half-duplex, bi-directional AUX CH PHY. The number of bus turn-around is reduced to minimize the half-duplex overhead.

The AUX CH PHY consists of a single differential pair carrying self-clocking data. All transactions shall start with a preamble "SYNC" for synchronizing Requester (Source Device) and Replier (Sink Device), and shall end with "STOP" condition.

A 4-bit command, COMM3:0, shall be transmitted after the preamble, followed by a 20-bit address, ADDR19:0. DisplayPort capability/status/control functions are directly mapped to the 20-bit address space. Furthermore, DisplayPort uses these 20 bits for accessing $I^2C$ devices.

After the transmission of command and address, data bytes shall be transmitted. Burst data transfer is supported. The burst data size shall be limited to 16 bytes or fewer.

This document also covers the mapping of $I^2C$ bus transactions to DisplayPort AUX CH, and provides some examples. Bit 3 (MSB) of the request command shall indicate whether the transaction is native DisplayPort or is a translated $I^2C$ transaction.

**Table 2.39 Bit/Byte Size of Various Data Types of AUX CH Syntax**

| Data Type | Bit Width |
|---|---|
| Command | 4 bits |
| Address | Request transaction: 20 bits |
| | Reply transaction: None (0000b shall be padded to Command to form a byte) |
| Data | Request transaction:<br>For read: 1 Byte (Length byte)<br>For write: 1Byte (Length byte) + N Data Bytes<br>- Length byte ("LEN") defines the number of bytes to be written to or to be read from AUX CH Replier (DisplayPort receiver, or Sink) by AUX CH Requester (DisplayPort transmitter, or Source).<br>- N = Integer value from 1 to 16. That is, Source Device is required to limit the burst data size to 16 bytes or fewer. |
| | Reply transaction:<br>For read = N Data bytes.<br>- N = Integer value from 1 to 16, the number of bytes ready to be sent out.<br>For write = 0 or 1 Data Byte<br>- When AUX CH Replier NACK's the write request transaction, it shall indicate how many bytes have been written to.<br>- For $I^2C$ write over AUX CH, AUX CH Replier, following ACK, shall indicate how many bytes have been written to the $I^2C$ slave. |

In the document, "►" is attached to a signal name that is driven by Requester, while "◄" to a signal driven by Replier.

### 2.4.1 Command definition

Request and reply command definitions of AUX CH transactions are described in this section.

#### *2.4.1.1 Request command definition*

bit 3 = Native AUX CH/ $I^2C$
1 = DisplayPort transaction, 0 = $I^2C$ transaction

When bit 3 = 1 (Native AUX CH transaction):

bits 2:0 = Request type
000 = Write, 001= Read

When bit 3 = 0 ($I^2C$ transaction):

bit 2 = MOT (Middle-of-Transaction) bit.

bits 1:0 = $I^2C$_Command

00 = Write, 01 = Read, 10 = Write Status_Request, 11 = Reserved

**Note**: More on MOT bit and I2C Write Status Request in Section 2.4.4.

#### *2.4.1.2 Reply command definition*

bits 3:0 = Reply type

0000 = ACK

- For Write transaction: Write completed
  - For DisplayPort write transaction: Has written all the data bytes.
  - For $I^2C$wrote transactions: Has written M bytes to $I^2C$ slave. ACK shall be followed by a data byte "M". When all the bytes have been written to and ACK'ed, the data byte "M" shall be omitted.
- For Read transaction: Ready to reply to Read request with data following.
  - Replier may assert STOP condition before transmitting the total number of requested data bytes, when not all the bytes are available.

0001 = NACK

- For Write transaction
  - Has written the first M bytes only. NACK shall be followed by a data byte,"M".
- For Read transaction
  - Does not have the requested data for the Read request transaction

0010 = DEFER

- For Write and Read transactions
  - Not ready for the Write/Read request. Retry later

0011 = Reserved

0100 = $I^2C$ NACK/AUX ACK

- Applicable to $I^2C$ transactions only:
  - For $I^2C$ Write transaction: Has written the first Mbytes to $I^2C$ slave before getting NACK. NACK shall be followed by a data byte "M".
  - For $I^2C$ Read transaction, $I^2C$ slave has NACK'ed the , $I^2C$ address.

1000 = $I^2C$ DEFER/AUX ACK

- Applicable to $I^2C$ transactions only:
  - For $I^2C$ Write and Read transactions: $I^2C$ slave has yet to ACK or NACK the $I^2C$ transaction.

1001 - 1111 = Reserved

### 2.4.2 Native AUX CH Request transaction syntax

SYNC► COMM3:0|ADDR19:16► ADDR15:8► ADDR7:0► LEN7:0► (DATA*0*-7:0► ....) STOP

#### *2.4.2.1 Write Request transaction*

- For write transaction (COMM3:0 = 1000), Request transaction shall stop when the number of bytes (1 - 16 = LEN7:0 value + 1, all other values are invalid) has been transmitted from Requester to Replier.

#### *2.4.2.2 Read Request transaction*

- For read transaction (COMM3:0 = 1001), Request transaction shall stop after LEN7:0. That is, no data shall be transmitted. Requester expects Replier to reply with [LEN7:0 value + 1] bytes (= 1 - 16 bytes)of data.

### 2.4.3 Native AUX CH Reply transaction syntax

SYNC◄ COMM3:0|0000 ◄ (DATA*0*-7:0◄... ) STOP

#### *2.4.3.1 Reply transaction to Write request*

Reply transaction to Write request shall end in one of the four conditions below:

- Replier has received a write request, and has completed the write. Replier shall reply the transaction by sending ACK.
  - SYNC◄ ACK|0000 ◄ STOP,
- Replier has received a write request, but has not completed the write. Replier shall end the transaction by sending NACK as the first COMM3:0, and then, the number of written bytes M as DATA0_7:0.
  - SYNC◄ NACK|0000 ◄ DATA*0*-7:0◄ STOP,
    where DATA*0*-7:0 shows the number of written bytes M

#### *2.4.3.2 Reply transaction to Read request*

Reply transaction to Read request shall end in one of the four conditions below:

- Replier has received a read request, but does not have the requested data in its Sink Device. Shall end the transaction by sending NACK as the first COMM3:0.

- SYNC◄ NACK|0000◄ STOP

- Replier has received a read request, but is not ready to reply with read data. Shall end the transaction by sending DEFER as the first COMM3:0.
  - SYNC◄ DEFER|0000◄ STOP
- Replier has received a read request, and is ready. Shall reply with ACK as the first command, transmit back the number of requested bytes, assert STOP condition, and release the AUX CH .
  - SYNC◄ ACK|0000 ◄ DATA*0*-7:0◄... DATA*N*-7:0◄ STOP
- Replier has received a read request, and is ready. Shall reply with ACK as the first command, but transmit only M bytes (M < requested number of bytes, N), assert STOP condition, and release the AUX CH.
  - SYNC◄ ACK|0000 ◄ DATA*0*-7:0◄... DATA*M*-7:0◄ STOP

### 2.4.4 $I^2C$ bus transaction mapping onto AUX CH Syntax

When bit 3 (MSB) of Request command is 0, the requested transaction shall be an $I^2C$ bus transaction. A single $I^2C$ may be divided into multiple AUX CH transaction, each with the bit 3 of the Request command set to 0.

In $I^2C$ bus transaction, the remaining 3 bits of the Request command are defined as follows:

- bit 2 = MOT (Middle-of-Transaction) bit.
  - This bit shall be set when the $I^2C$ transaction does not end (or STOP) with the current AUX CH transaction. The $I^2C$ master in DisplayPort receiver shall send out the 7-bit I2C address and R/W command only when:
    - MOT bit is set to 1 for the first time, that is, in the first AUX CH transaction for the START of I2C transaction,
      or
    - RepeatedSTART is issued, which results either in a new I2C address. or the same I2C address but the R/W command is reversed.
- bits 1:0 = $I^2C$_Command
  - 00 = Write
  - 01 = Read
  - 10 = Write_Status_Request
    - When the last $I^2C$ Write transaction resulted in a reply of either $I^2C$_DEFER or ACK followed by a data byte "M" where M is the number of bytes written to the $I^2C$ slave, AUX CH Requester (DisplayPort transmitter) may issue the following special request to inquire the status of the last $I^2C$ write:

      SYNC► COM3:0 (= 0110)|0000► 0000|0000► 0|7-bit $I^2C$ address (the same as the last) ► 0000|0000 (Length byte) ► STOP►

    - To this request, AUX CH Replier (DisplayPort receiver) shall reply wit the latest status.
  - 11 = Reserved

### *2.4.4.1 Streaming I²C Transactions*

In many practical configurations, the DisplayPort AUX CH may bridge I²C bus in the Source device and another I²C bus in the Sink Device as shown in Figure 2.31.

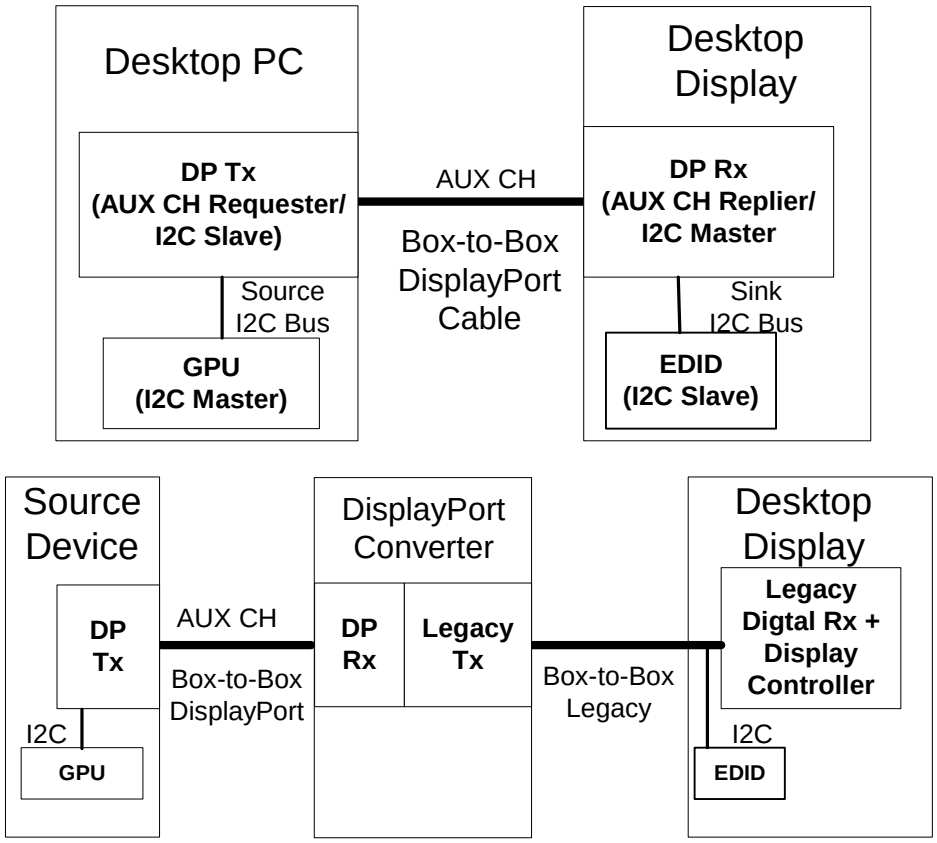



**Figure 2.31 Examples of AUX CH Bridging Two I²C Buses**

In these configurations, there are two separate I²C buses: First between GPU and DisplayPort Tx, the second between DisplayPort Rx (and Legacy Tx) and EDID.

DisplayPort transmitter shall act as I²C slave in the Source device while DisplayPort receiver shall act as I²C master in the Sink Device. Since the data rate of those two I²C buses are likely to be different, "streaming control" of I²C transactions shall be required.

#### 2.4.4.1.1 Example of EDID read over AUX CH

The example of I²C transactions and AUX CH transactions that take place when an I²C master in Source Device (for instance, GPU) initiates an EDID read transaction by issuing an I²C write command to EDID ROM (that is, A0h) in Sink Device is shown below. "►" indicates that the signal is directed from Master to Sink (or Requester to Replier) while "◄" indicates the opposite direction.

I²C write transaction by GPU

START► 1010 000|0 (A0h)► ACK◄ Data0 (Address Offset)► ACK◄ RepeatedStart►
*Clock Stretch by I²C slave in DisplayPort Transmitter*

AUX CH write request transaction by DisplayPort transmitter

SYNC► 0100|0000 ($I^2C$ write, MOT bit = 1)► 0000|0000► 0|101 0000 (7-bit $I^2C$ address for EDID)► Data0 (Address Offset) )►STOP►

$I^2C$ write transaction by DisplayPort receiver to EDID ROM

START► 1010 000|0 (A0h)► ACK◄ Data0 (Address Offset) )► ACK◄

AUX CH reply transaction by DisplayPort receiver

SYNC◄ 0000|0000 (ACK)◄ STOP◄

$I^2C$ read transaction by GPU

START► 1010 000|1 (A1h)► *Clock Stretch by in DisplayPort transmitter*

AUX CH read request transaction by DisplayPort transmitter

SYNC► 0101|0000 ($I^2C$ read transaction, MOT = 1)► 0000|0000►
0|101|0000 (7-bit $I^2C$ address for EDID) ► 0000|1111 (Length, pre-fetching 16 bytes)► STOP►

$I^2C$ read transaction by DisplayPort receiver

START► 7-bit I2C Address|1► ACK◄ Data1◄ ACK► Data2◄ ACK► …. Data8◄ ACK► *DisplayPort receiver continues $I^2C$ read from its $I^2C$ slave.*

AUX CH reply transaction by DisplayPort receiver upon AUX CH time-out (200us)

SYNC◄ 0000|0000 (ACK)◄ Data1◄ Data2◄ Data3◄ Data4◄ Data5◄ Data6◄ Data7◄ Data8◄ STOP◄

$I^2C$ read transaction by GPU

*Clock line released by DP Tx* ACK◄ Data0◄ ACK► … Data8◄ ACK► *Clock stretched by DisplayPort transmitter*

AUX CH read request transaction by DisplayPort transmitter

SYNC► 0101|0000 ($I^2C$ read transaction, MOT = 1)► 0000|0000►
0|101|000 (7-bit I2C Address for EDID)► 0000|1111(Length = 16 bytes, requesting 16 more bytes, Data9 - Data24)► STOP►

$I^2C$ read transaction by DisplayPort receiver

… Data14◄ ACK► Data15◄ ACK► ….Data22◄ ACK► *DisplayPort receiver continues $I^2C$ read from its I2C slave.*

AUX CH reply transaction by DisplayPort receiver upon AUX CH time-out

SYNC◄ 0000|0000◄ (ACK = Read data ready) Data9◄ Data10◄… Data22◄ STOP◄.

$I^2C$ read transaction by GPU

*Clock line released by DP Tx* ACK◄ Data9◄ ACK► … Data22◄ ACK► *Clock stretched by DP Tx*

The transactions continue…

AUX CH read request transaction by DisplayPort transmitter (after received Data 120)

SYNC► 0001|0000 (I2C read transaction, MOT = 0)► 0000|0000►
0|101|0000)► 0000|0111(Length = 8 byte, requesting 8 bytes from Data 121)► STOP►

$I^2C$ read transaction by DisplayPort receiver

… Data126◄ ACK► Data127◄ ACK► Data128◄ NACK► STOP ►

AUX CH reply transaction by DisplayPort receiver upon AUX CH time-out

SYNC◄ 0000|0000◄ (ACK = Read data ready) Data121◄ Data122◄… Data128◄ STOP◄.

$I^2C$ read transaction by GPU

*Clock line released by DP Tx* ACK◄ Data121◄ ACK► … Data128◄ NACK► STOP►

### *2.4.4.2 $I^2C$ ACK/NACK*

The $I^2C$ ACK does not guarantee data integrity of an $I^2C$ transaction. The data integrity shall be confirmed by an upper layer on top of $I^2C$ bus. The $I^2C$ ACK, however, serves another purpose: It confirms the presence of $I^2C$ device at the specified address.

When DisplayPort AUX CH is bridging two $I^2C$ buses, the following rule shall be followed for ACK/NACK response to $I^2C$ commands:

- DisplayPort transmitter shall acknowledge the $I^2C$ command, unless it is certain it does not support the specified $I^2C$ address or the corresponding AUX CH transaction is NACK'ed by DisplayPort receiver.
- DisplayPort receiver shall acknowledge the AUX CH transaction, unless it is certain it does not support the specified $I^2C$ address.

By following the above rule, the $I^2C$ master in the Source Device is able to avoid issuing the $I^2C$ command to the same $I^2C$ address infinitely.

Table 2.40 shows the list of addresses to be supported by DisplayPort transmitter. Support of additional $I^2C$ address (to which $I^2C$ ACK is generated) is an implementation decision.

**Table 2.40 Minimum Set of $I^2C$ Addresses ACK'ed by DisplayPort**

| $I^2C$ Slave Address | Devices |
|---|---|
| 60h | E-EDID for setting segment beyond the 1st 256 bytes |
| 6Eh/6Fh | DDC/CI |
| A0h/A1h | EDID |

## 2.5 AUX CH Services

This section describes two types of AUX CH services, AUX CH Link Services and AUX CH Device Services. These are the Link Layer services used by "Policy Makers" for link and device management both in the Source Device and the Sink Device.

Whenever the Hot Plug Detect signal is active (the connectors are plugged in and the Sink Device has at least a "trickle" AC power), AUX CH services shall be available.

There are two Policy Makers.

- Stream Policy Maker
  - Manages stream
    - Stream transport initialization, and maintenance
      (More on this subject is covered in the following sections)
    - Uses AUX CH Device Services
    - Gets link information from Link Policy Maker
- Link Policy Maker
  - Manages link
    - Link discovery, initialization, and maintenance
    - Uses AUX CH Link Services

Both Source and Sink Devices shall have these two policy makers. Policy Makers may be implemented as Operating System, software driver, firmware, or hardware state machine. The choice is implementation specific. In this document, only the semantics of interface between Link Layer and Policy Makers is defined: Syntax (i.e., API) is implementation specific, and is not covered in DisplayPort specification.

### 2.5.1 Stream Transport Initiation Sequence

Stream Source Policy Maker, before transport initiation, shall take the following action:

- Read EDID from the Sink Device
- Set stream attributes for Main Stream Attribute data and CEA861-C InfoFrame generation
- Optionally (recommended), get the following info. from Link Policy Maker
  - Link configuration: Total link bandwidth
    - For avoiding oversubscription of the link bandwidth
  - Rx capability: Number and types of ports available in Rx
    - For determining the number and types of streams that may be transported
  - Link status: Synchronized? Excessive error symbols?
    - For making sure that link is ready for transport
- When a stream is ready for transport, Stream Source Policy Maker shall start the transport of isochronous stream along with stream attributes data.

Stream sink, upon receiving stable stream, shall decode stream attributes data, and start reconstructing the incoming isochronous stream.

Stream Source Policy Maker may incorporate the link capability information for the stream source management: DisplayPort-aware Stream Source Policy Maker, for example, may try to limit the stream bandwidth equal to or below available link bandwidth, thus preventing link bandwidth over-subscription. If a stream is going to oversubscribe the link bandwidth, the Stream Source Policy Maker may inform the stream source. The stream source, upon receiving this notice, may take a corrective action, such as the reduction of image resolution and/or color depth (in bits per pixel).

Though it is desirable, such an interaction between two Policy Makers is optional. In other words, DisplayPort Link shall be implemented to function with a legacy Source Policy Maker that is unaware of DisplayPort.

Diagrams of a typical action flow of the Source Device and the Sink Device upon Hot Plug Detect event are shown in Figure 2.32. Note that the diagrams are examples only. It is not required, for instance, that EDID read precede DPCD read.

Also note that above diagram shows a typical action flow for a consumer-detachable, box-to-box DisplayPort connection. When DisplayPort is used for embedded connection, such as from a GPU to a notebook panel TCON within notebook PC, DPCD read may not be needed. In this embedded configuration, the Source (GPU) may, instead, use pre-set link capability information of the DisplayPort receiver.

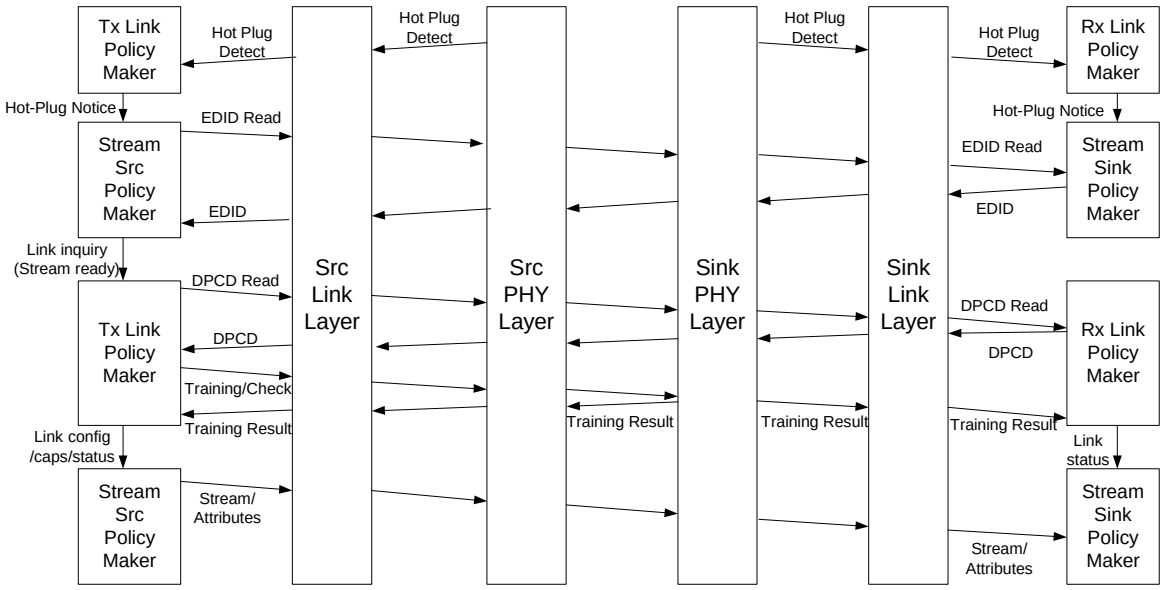



**Figure 2.32 Action flow sequences of the Source upon Hot Plug Detect event (INFORMATIVE)**

### 2.5.2 Stream Transport Termination Sequence

Examples of events causing stream termination are as follows:

- Link error event notice by Link Policy Maker
- Stream timing change
- Stream format change, unstable stream timing, loss of stream

Stream Source shall terminate the transport of Main Stream and Secondary data. It may re-initiate the transport following the initiation sequence once link is re-established. As far as the Stream Sink is concerned, the recommended correction action is either to display blank screen/alert message or to turn off the display until stable stream reception is resumed.

### 2.5.3 AUX CH Link Services

In order to transport isochronous data stream from Source Device to Sink Device, Link Policy Maker shall first establish the Main Link. The Main Link shall be established in the following steps in sequence. Note that all the commands are memory mapped, whether setting or getting link parameters. The address mapping is shown Table 2.41 in this section.

**Step_1:** Unless it has a pre-set knowledge, the Source shall initiate **Link Discovery**, by reading Link Capability field of DPCD through AUX CH. The Link Capability field shall describe the link capability of the DisplayPort receiver in the Sink Device, such as main link maximum bit rate and main link maximum number of lanes. More detail on reading DPCD is explained later in this section.

**Step_2:** Based on the DPCD information, Source shall start **Link Initialization** process. The following sequences shall take place during Link Initialization:

- Link Policy Maker in the Source Device shall start Link Training. This function call shall notify the Sink of the ensuing transport of training pattern through Main Link PHY layer, with link configuration and training attributes defined in this function.
- Link Policy Maker shall check the training status and report of final results.

If the Link Policy Maker detects a failed link training attempt, it shall take corrective action. Possible correction actions are:

- Reduction of the bit rate if link was in the high bit rate mode,
- Termination of Link Initialization

This loop of setting Main Link configuration and forwarding training pattern, while checking the status shall end with final result of either pass or fail. "Pass" means that the bit lock and symbol lock have been achieved on each of the configured lanes, and all the lanes are symbol locked, and properly inter-lane aligned (with skew of two LS_Clk period between adjacent lanes). Otherwise, it is "fail".

**Step_3**: If a receiver is capable of de-spreading as indicated in DPCD, then the Source may optionally get the Time Stamp N for de-spreading from the Sink, if de-spreading is needed.

After the Main Link is established, the Link Policy Maker of Source Device shall check the link status whenever it detects the HPD (Hot Plug Detect) signal toggle after the rising edge of HPD. Source Device shall ignore low or high pulse period of less than 0.25 ms. In other words, Source Device will not check the link status until at least 0.25 ms after the rising edge.

The Sink Device shall clear the HPD signal to low level for 0.5 ms to 1 ms before setting it high again whenever there is a status change either in the link or in the device in order to notify Source device of the status change.

Source Device shall check Link Status field of DPCD (as described in Table 2.41) through AUX CH read transaction to identify the cause within 100 ms after the rising edge of HPD. Upon identifying the cause, the Link Policy Maker shall take corrective action.

**INFORMATIVE NOTE:** In case the HPD signal toggling (or bouncing) is the result of the Hot Unplug followed by Hot Plug of a cable-connector assembly, then the HPD signal is likely to remain unstable during the debouncing period, which is in the order of tens of ms. Source Device may either check the stability of the HPD signal before initiating AUX CH read transaction or immediately initiate the AUX CH read transaction after each HPD rising edge.

### *2.5.3.1 Address Mapping for Link Configuration/Management*

Table 2.41 shows the DisplayPort Address Mapping for DPCD. The DPCD is byte addressed.

**Table 2.41 Address Mapping for DPCD (DisplayPort Configuration Data)**

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| ***Receiver Capability Field*** | | |
| 00000h | DPCD_REV<br>DPCD revision number<br>Bits3:0 = Minor Revision Number<br>Bits7:4 = Major Revision Number<br><br>10h for DPCD Rev.1.0<br><br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common revision number shall be used.* | Read Only |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| 00001h | MAX_LINK_RATE<br>Bits7:0 = MAX_LINK_RATE<br>Maximum link rate of Main Link lanes<br>= Value x 0.27Gbps per lane<br><br>For DisplayPort Ver.1.0, only two values supported. All other values are reserved.<br>06h = 1.62Gbps per lane<br>0Ah = 2.7Gbps per lane<br><br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common link rate shall be used* | Read Only |
| 00002h | MAX_LANE_COUNT<br>Bits4:0 = MAX_LANE_COUNT<br>Maximum number of lanes = Value<br><br>For Rev.1.0, only the following three values are supported. All other values are reserved.<br>1h = One lane<br>2h = Two lanes<br>4h = Four lanes<br><br>For one-lane configuration, Lane0 is used. For 2-lane configuration, Lane0 and Lane1 are used.<br><br>Bits7:5 = RESERVED. Read all 0's.<br><br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common lane count shall be used.* | Read Only |
| 00003h | MAX_DOWNSPREAD<br>Bit 0 = MAX_DOWNSPREAD<br>0 – No spread supported<br>1 – 0.5% down spread<br><br>Bits7:1 = RESERVED. Read all 0's.<br><br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common down-spread value shall be used.* | Read Only |
| 00004h | NORP<br>Bits0 = NORP<br>Number of Receiver Ports = Value<br><br>For DisplayPort Rev.1.0, the maximum number is two, one for an | Read Only |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| | uncompressed video stream and the other for its associated audio stream. The receiver can simultaneously receive up to "NORP" isochronous streams.<br><br>Smallest available Receiver Port number is assigned. For example, when there is only one receiver port, the receiver port is assigned to ReceiverPort0. ReceiverPort1 shall be assigned only after Receiver Port 0 has already been assigned.<br><br>Bits7:1 = RESERVED. Read all 0's. | |
| 00005h | DOWNSTREAMPORT_PRESENT<br>Bit 0 = DWN_STRM_PORT_PRESENT<br>Set to 1 when this device has downstream port(s)<br><br>***Note**: This bit is set to 1 only in Branch Device.*<br><br>Bits 2:1 = DWN_STRM_PORT_TYPE<br>Indicates the downstream port type<br>00 = DisplayPort<br>01 = Analog VGA or analog video over DVI-I<br>10 = DVI or HDMI<br>11 = Others (This downstream port type will have no EDID in Sink Device: For example, composite video and Svideo ports)<br><br>Bits7:3 = RESERVED. Read all 0's. | Read Only |
| 00006h | MAIN_LINK_CHANNEL_CODING<br>Bit 0 = ANSI8B10B<br>This bit set to 1 when DisplayPort receiver supports the Main Link channel coding specification as specified in ANSI X3.230-1994, clause 11.<br><br>Bits 7:1 + RESERVED. Read all 0's. | |
| 00007h | RESERVED | Reads all 0's |
| 00008h | RECEIVE_PORT0_CAP_0<br>ReceiverPort0 Capability_0<br>Bit0 = RESERVED. Read 0<br><br>Bit1 = LOCAL_EDID_PRESENT<br>1 = This receiver port has a local EDID.<br>0 = This receiver port has no local EDID.<br><br>***Note**: "Sink Device" and "Format Converter" shall have a local EDID.*<br><br>Bit2 = ASSOCIATED_TO_PRECEDING_PORT | Read Only |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| | 1 = This port is used for secondary isochronous stream of main stream received in the preceding port<br>0 = This port is used for main isochronous stream. This bit shall always be zero for Receiver Port 0.<br><br>Bits7:3 = RESERVED. Read all 0's.<br>***Note**: For Receiver Port0, this bit 3 shall be 0.* | |
| 00009h | RECEIVE_PORT0_CAP_1<br>ReceiverPort0 Capability_1<br>Bits7:0 = BUFFER_SIZE<br>Buffer size = (Value+1) * 32 bytes per lane<br><br>The maximum is 8Kbytes per lane. | Read Only |
| 0000Ah | RECEIVE_PORT1_CAP_0<br>ReceiverPort1 Capability_0<br>Bit definition is identical to that of RECEIVE_PORT0_CAP_0.<br><br>***Note**: When Receiver Port 1 not present, reads all 0's.* | Read Only |
| 0000Bh | RECEIVE_PORT1_CAP_1<br>ReceiverPort1 Capability_1<br>Bit definition is identical to that of REDEIVE_PORT0_CAP_1.<br><br>***Note**: When Receiver Port 1 not present, reads all 0's.* | Read Only |
| 0000Ch<br>- 000FFh | RESERVED | Reads<br>all 0's |
| ***Link Configuration Field*** | | |
| 00100h | LINK_BW_SET<br>Bits7:0 = LINK_BW_SET<br>Main Link Bandwidth Setting=Value x 0.27Gbps per lane<br><br>For DisplayPort Rev.1.0, only two values supported. All other values are reserved.<br>06h = 1.62Gbps per lane<br>0Ah = 2.7Gbps per lane<br><br>Source may choose either of the two link bandwidth as long as it does not exceed the capability of DisplayPort receiver as indicated in the receiver capability field. | Write/Read |
| 00101h | LANE_COUNT_SET<br>Bits4:0 = LANE_COUNT_SET<br>Main Link Lane Count = Value<br><br>For DisplayPort Rev.1.0, only the following three values are supported. All other values are reserved.<br>1h = One lane | Write/Read |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| | 2h = Two lanes<br>4h = Four lanes<br><br>For one-lane configuration, Lane0 is used. For 2-lane configuration, Lane0 and Lane1 are used. Source may choose any lane count as long as it does not exceed the capability of DisplayPort receiver as indicated in the receiver capability field.<br><br>Bits7:5 = RESERVED. Read all 0's. | |
| 00102h | TRAINING_PATTERN_SET<br>Bits1:0 = TRAINING_PATTERN_SET<br>Link Training Pattern Setting<br>00 – Training not in progress (or disabled)<br>01 – Training Pattern 1<br>10 – Training Pattern 2<br>11 – RESERVED<br><br>Bits3:2 = LINK_QUAL_PATTERN_SET<br>00 – Link quality test pattern not transmitted<br>01 – D10.2 test pattern (unscrambled) transmitted (same as Training Pattern 1)<br>10 – Symbol Error Rate measurement pattern transmitted<br>11 – PRBS7 transmitted<br><br>Bit 4 = RECOVERED_CLOCK_OUT_EN<br>0 – Recovered clock output from a test pad of DisplayPort Rx not enabled<br>1 – Recovered clock output from a test pad of DisplayPort Rx enabled.<br><br>Bit 5 = SCRAMBLING_DISABLE<br>0 – DisplayPort transmitter scrambles data symbols before transmission<br>1 – DisplayPort transmitter disables scrambler and transmits all symbols without scrambling<br><br>Bits7:6 = RESERVED. Read all 0's. | Write/Read |
| 00103h | TRAINING_LANE0_SET<br>Link Training Control_Lane0<br>Bits1:0 = DRIVE_CURRENT_SET<br>00 – Training Pattern 1 w/ drive current level 0<br>01 – Training Pattern 1 w/ drive current level 1<br>10 – Training Pattern 1 w/ drive current level 2<br>11 – Training Pattern 1 w/ drive current level 3<br><br>Bit2 = MAX_CURRENT_REACHED | Write/Read |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| | Set to 1 when the maximum driven current setting is reached.<br><br>***Note**: Transmitter shall at least three levels of drive current corresponding to the differential voltage swing of 400mV- 600mV-, and 800mV_diff_pp. If only three levels of drive current is supported, then program Bit 2 shall be set to 1 when Bits 1:0 are set to 10.*<br><br>Bit4:3 = PRE-EMPHASIS_SET<br>00 = Training Pattern 2 w/o pre-emphasis<br>01 = Training Pattern 2 w/ pre-emphasis level 1<br>10 = Training Pattern 2 w/ pre-emphasis level 2<br>11 = Training Pattern 2 w/ pre-emphasis level 3<br><br>Bit5 = MAX_PRE-EMPHASIS_REACHED<br>Set to 1 when the maximum drive current setting is reached.<br><br>***Note**: Transmitter shall support at least two levels of pre-emphasis (3.5dB and 6dB) in addition to no pre-emphasis (0dB). Support of additional pre-emphasis level is optional. If only 0dB, 3.5dB, and 6dB are supported, the transmitter shall set bit5 when it sets bits4:3 to 2h (level2), to indicate to the receiver that the maximum pre-emphasis level has been reached. Support of independent pre-emphasis level control for each lane is also optional.*<br><br>Bits7:6 = RESERVED. Read all 0's. | |
| 00104h | TRAINING_LANE1_SET<br>(Bit definition identical to that of TRAINING_LANE0_SET.) | Write/Read |
| 00105h | TRAINING_LANE2_SET<br>(Bit definition identical to that of TRAINING_LANE0_SET.) | Write/Read |
| 00106h | TRAINING_LANE3_SET<br>(Bit definition identical to that of TRAINING_LANE0_SET.) | Write/Read |
| 00107h | DOWNSPREAD_CTRL<br>Down-spreading control<br>Bit 0 = MODULATION_FREQ<br>Spread spectrum modulation frequency<br>0 – 30kHz<br>1 – 33kHz<br><br>Bit 3:1 = RESERVED. Read all 0's<br><br>Bits 4 = SPREAD_AMP<br>Spreading amplitude<br>0 – 0.0% down spread<br>1 – 0.5% down spread<br><br>Bit 7:5 = RESERVED. Read all 0's. | Read/Write |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| | ***Note**: Write 00h to declare to the receiver that there is no down-spreading.* | |
| 00108h | MAIN_LINK_CHANNEL_CODING_SET<br>Bit 0 = SET_ANSI8B10B<br>This bit selects the Main Link channel coding specification as specified in ANSI X3.230-1994, clause 11.<br><br>Bits 7:1 = RESERVED. Read all 0's. | |
| 00109h<br>- 001FFh | RESERVED | Reads<br>all 0's |
| ***Link/Sink Status Field*** | | |
| 00200h | SINK_COUNT<br>Sink Device count<br><br>Bits5:0 = SINK_COUNT<br>Total number of the Sink Devices within this device and those connected to the downstream ports of this device<br><br>***Note**: Branch Device shall add up the Rendering Function counts read from all of its downstream ports. It shall add one more if it has a local Rendering Function. The maximum number of Rendering Function count in a link shall be limited to 32 or fewer. This limitation is enforced by the DPCP.*<br><br>Bit6 = CP_READY<br>Set to 1 when all of Sink Devices (local Sink and those connected to its downstream ports) are CP-capable. This bit shall be set at the conclusion of Content Protection Authentication.<br><br>***Note**: Source Device shall transmit a content that requires content protection only when all the Branch and Sink Devices in the link are CP-ready except for Repeater Device. (Repeater Device is not required to perform DPCP decryption/encryption operation, and therefore is not required to be CP-ready.) DPCP specification shall define the method with which to notify users of this limitation.*<br><br>Bits7 = RESERVED | Read only |
| 00201h | DEVICE_SERVICE_IRQ_VECTOR<br>Bit 0 = RESERVED for REMOTE_CONTROL_COMMAND_PENDING<br>When this bit is set to 1, Source Device shall read the Device Services Field for REMOTE_CONTROL_COMMAND_PASS_THROUGH.<br><br>Bit 1 =RESERVED for AUTOMATED_TEST_REQUEST<br>When this bit is set to 1, Source Device shall read Addresses 00218h - 0025Fh for requested link test. | Read only |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| | Bits 5:2 = RESERVED. Read 0.<br><br>Bit 6 =SINK_VENDOR_SPECIFIC_IRQ<br>Usage is vendor-specific.<br><br>Bit 7 = RESERVED. Read 0. | |
| 00202h | LANE0_1_STATUS<br>Lane0 and Lane1 Status<br>Bit 0 = LANE0_CR_DONE<br><br>Bit 1 = LANE0_CHANNEL_EQ_DONE<br><br>Bit 2 = LANE0_SYMBOL_LOCKED<br><br>Bit 3 = RESERVED. Read 0.<br><br>Bit 4 = LANE1_CR_DONE<br><br>Bit 5 = LANE1_CHANNEL_EQ_DONE<br><br>Bit 6 = LANE1_SYMBOL_LOCKED<br><br>Bit 7 = RESERVED. Read 0. | Read only |
| 00203h | LANE2_3_STATUS<br>(Bit definition identical to that of LANE0_1_STATUS) | Read only |
| 00204h | LANE_ALIGN__STATUS_UPDATED<br>Bit 0 = INTERLANE_ALIGN_DONE<br><br>Bits 5:1 = RESERVED. Read all 0's.<br><br>Bit 6 = DOWNSTREAM_PORT_STATUS_CHANGED<br>Bit 6 is set when any of the downstream ports has changed status.<br><br>Bit 7 = LINK_STATUS_UPDATED<br>Link Status and Adjust Request updated since the last read. Bit 7 is set when updated and cleared after read. | Read only |
| 00205h | SINK_STATUS<br>Bit 0 = RECEIVE_PORT_0_STATUS<br>0 = SINK out of sync<br>1 = SINK in sync<br><br>Bit 1 = RECEIVE_PORT_1_STATUS<br>0 = SINK out of sync<br>1 = SINK in sync | |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| | Bits 7:2 = RESERVED. Read all 0's | |
| 00206h | ADJUST_REQUEST_LANE0_1<br>Drive Current and Equalization Setting Adjust Request for Lane0 and Lane1<br>Bits 1:0 = DRIVE_CURRENT_LANE0<br>00 = Level 0, 01 = Level 1, 10 = Level 2, 11 = Level 3<br><br>Bits 3:2 = PRE-EMPHASIS_LANE0<br>00 = Level 0, 01 = Level 1, 10 = Level 2, 11 = Level 3<br><br>Bits 5:4 = DRIVE_CURRENT_LANE1<br>00 = Level 0, 01 = Level 1, 10 = Level 2, 11 = Level 3<br><br>Bits 7:6 = PRE-EMPHASIS_LANE1<br>00 = Level 0, 01 = Level 1, 10 = Level 2, 11 = Level 3 | Read only |
| 00207h | ADJUST_REQUEST_LANE2_3<br>(Bit definitions as in ADJUST_REQUEST_LANE0_1) | Read only |
| 00208h | TRAINING_SCORE_LANE0<br>Reserved for DisplayPort Ver.1.0. Read 0. | Read only |
| 00209h | TRAINING_SCORE_LANE1<br>Reserved for DisplayPort Ver.1.0. Read 0. | Read only |
| 0020Ah | TRAINING_SCORE_LANE2<br>Reserved for DisplayPort Ver.1.0. Read 0. | Read only |
| 0020Bh | TRAINING_SCORE_LANE3<br>Reserved for DisplayPort Ver.1.0. Read 0. | Read only |
| 0020Ch<br>- 0020Fh | RESERVED | Read all 0's |
| 00210h<br>- 00211h | SYMBOL_ERROR_COUNT_LANE0<br>15-bit value storing the symbol error count of Lane 0<br>00210h bits7:0= Error Count Bits7:0<br>00211h bits6:0 = Error Count Bits14:8<br>00211h bit7 = Error count valid<br>Set to 1 when the error count value is valid.<br><br>These bytes hold a 15-bit value only when LINK_QUAL_PATTERN_SET in TRAINING_PATTERN_SET byte is set to 10 (binary). The 15-bit value is cleared upon AUX_CH read by a transmitter | Read only |
| 00212h<br>- 00213h | SYMBOL_ERROR_COUNT_LANE1<br>15-bit value storing the symbol error count of Lane 1<br>00212h bits7:0= Error Count Bits7:0<br>00213h bits6:0 = Error Count Bits14:8<br>00213h bit7 = Error count valid<br>Set to 1 when the error count value is valid. | Read only |

| DisplayPort Address | Definition | Read/Write over AUX CH |
|---|---|---|
| 00214h<br>- 00215h | SYMBOL_ERROR_COUNT_LANE2<br>15-bit value storing the symbol error count of Lane 2<br>00214h bits7:0= Error Count Bits7:0<br>00215h bits6:0 = Error Count Bits14:8<br>00215h bit7 = Error count valid<br>Set to 1 when the error count value is valid. | Read only |
| 00216h<br>- 00217h | SYMBOL_ERROR_COUNT_LANE3<br>15-bit value storing the symbol error count of Lane 3<br>00216h bits7:0= Error Count Bits7:0<br>00217h bits6:0 = Error Count Bits14:8<br>00217h bit7 = Error count valid<br>Set to 1 when the error count value is valid. | Read only |
| 00218h<br>- 0027Fh | RESERVED for automated link testing purpose. | Read all 0's |
| 00280h<br>- 002FFh | RESERVED | |
| ***Vendor-Specific Field for Source Device*** | | |
| 00300h<br>- 003FFh | RESERVED for Source vendor-specific usage. | |
| ***Vendor-Specific Field for Sink Device*** | | |
| 00400h<br>- 004FFh | RESERVED for Sink vendor-specific usage | |
| ***Vendor-Specific Field for Branch Device*** | | |
| 00500h<br>- 005FFh | RESERVED for Branch Device vendor-specific usage | |
| ***Usage to be defined*** | | |
| 00600h<br>- 6FFFFh | RESERVED | Read all 0's |
| ***Usage to be defined*** | | |
| 70000h<br>- 77FFFh | RESERVED for DPCP specification. | Read only |
| 78000h<br>- 7FFFFh | RESERVED for DPCP specification | Write/Read |

### *2.5.3.2 DPCD in Multi-Hop Topology*

DisplayPort link has multiple hops when one or more Sink Devices connected to Source Device via Branch Device(s). When multiple hops of DisplayPort constitutes either daisy-chain or tree topology, the DPCD of the Branch Device shall comprehend DPCD(s) of its downstream links. Upstream DisplayPort device shall check only the DPCD of its immediate downstream device regardless of the link topology.

For behaviors of Branch Device upon detecting the status change of the downstream ports, refer to Section 5.3.2 on p.199.

#### 2.5.3.2.1 Receiver Capability of Downstream Legacy Link

Generally speaking, a legacy link does not have a link capability field equivalent to that defined for DPCD. Capabilities vary: Some legacy link can support both audio and video, while the others are limited to video only. Supported pixel data rate and color format are also dependent on the type of legacy link and its implementation.

DisplayPort Source Device, when connected to a legacy Sink Device via DisplayPort-to-legacy converter, shall determine the stream format based solely on the Sink Device capability expressed in the EDID of the legacy Sink Device.

### *2.5.3.3 Link Initialization through Link Training*

DisplayPort link initialization (before transporting a stream) shall be needed unless the Source Main Link transmitter and the Sink Main Link receiver are already in synchronization as indicated in Link Status field. During link initialization AUX CH services shall be used to train the link with a desired set of link configuration parameters. For detailed description of Link Training sequence, refer to Section 3.4.1.3 starting from 128.

After Link Training is successfully completed before the transport of a main video stream starts, the Source Main Link transmitter shall be sending "idle pattern" consisting of BS symbol set (BS symbol followed by VB-ID with its NoVideoStream_Flag set to 1) inserted every $2^{13}$ (or 8,192) link.

Source Device shall start sending the idle pattern after it has cleared the Training_Pattern byte in DPCD. Sink Device, should be ready to receiving the "idle pattern" as soon as it updates the link status field of DPCD to indicate the successful completion of Link Training to Source Device.

For closed, embedded connection, DisplayPort transmitter and receiver may be set to pre-calibrated parameters without going through the full link training sequence. In this mode, DisplayPort transmitter may start a normal operation following the transmission of Clock Recovery Pattern with pre-calibrated drive current and pre-emphasis level, as shown with a dotted arrow in Figure 2.33.

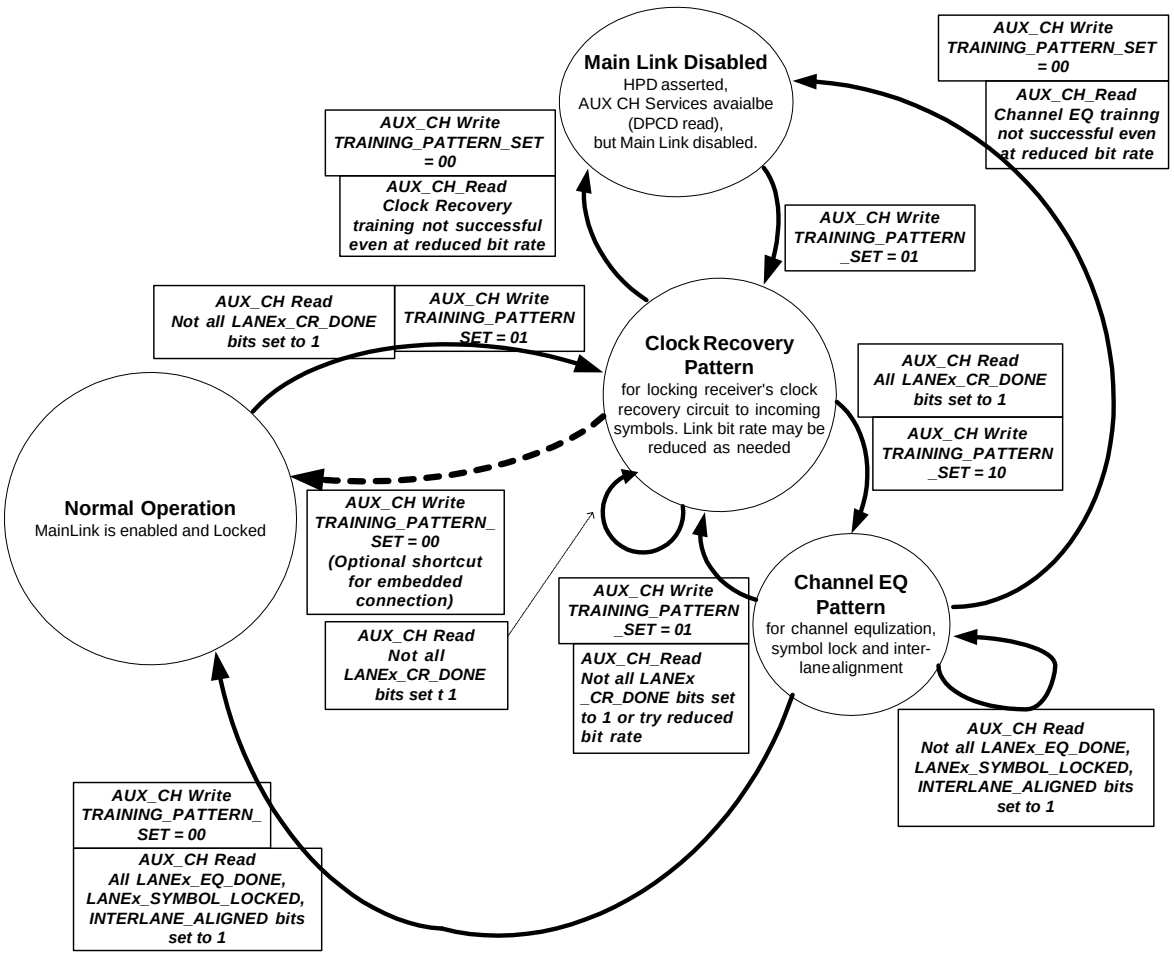



**Figure 2.33 Link Training State**

### *2.5.3.4 Link Maintenance*

Link Policy Maker of Source Device shall check the link status whenever it detects the IRQ HPD signal toggle within 100 ms after the rising edge of the HPD for possible Main Link synchronization loss. This check is performed by reading the Link Status field of DPCD, addresses 00200h – 00205h

Note that a format change in the transported stream does not necessarily result in Link Status change as long as the link stays stable. For example, some Source Devices may choose to continue transmitting stuffing symbols when the stream has stopped. In this case, the Main Link stays synchronized

### *2.5.3.5 Link Quality Test Support*

DisplayPort supports a test procedure for measuring the link quality. The following features are supported:

- Transmission of Nyquist pattern (repetition of D10.2 symbols without scrambling)
- Symbol Error measurement pattern

#### 2.5.3.5.1 Transmission of Nyquist Pattern

This pattern consists of repetition of D10.2 symbols (without scrambling), identical to the Training Pattern 1 for Bit-lock. This pattern results in the Main Link toggling at the highest frequency (for example, 1.35GHz when the link bit rate is 2.7Gbps). System integrator may use this pattern to measure, for example, the jitter performance of the transmitted signals.

The DisplayPort Source Device signals the transmission of this pattern by writing 01 to bits 3:2 of TRAINING_PATTERN_SET byte.

Upon being notified of the transmission of this pattern, the DisplayPort Sink Device shall blank its screen while keeping the DisplayPort receiver running.

#### 2.5.3.5.2 Symbol Error Rate Measurement Pattern

This pattern consists of repetition of data 00h that gets scrambled by a transmitter. (As for the polynomial for this scrambling, refer to Section 3.4.1.1 on p.122.) The DisplayPort Source Device shall periodically (every $2^{13}$ or 8192 symbols) transmit BS symbol. The Physical Layer shall replace every $512^{th}$ BS with BR symbol to reset the scrambler.

Upon being notified of the transmission of this pattern, the DisplayPort Sink Device shall start increasing the SYMBOL_ERROR_COUNT_LANEx value each time it has unscrambled a non-00h data value.

The DisplayPort Source Device shall read the SYMBOL_ERROR_COUNT_LANEx values some time later. Using the read values and elapsed time, it shall calculate the rough estimate of the symbol error rate.

Transmitting 1E+9 link symbols roughly takes 10 seconds. Therefore, the transmitter is recommended to wait for 10 to 100 seconds before reading the Symbol Error count from a receiver.

Symbol error rate is calculated as follows:

- At 2.7Gbps:
  - Symbol Error Rate in unit of $10^{-9}$
    = Error_Count/ (0.27 * Measurement Period in second)
- At 1.62Gbps:
  - Symbol Error Rate in unit of $10^{-9}$
    = Error_Count/ (0.62 * Measurement Period in second)

### 2.5.4 AUX CH Device Services

Aux Device Services are used for the purpose of communication between Graphic host and display device. The following are examples of display device services that are supported by Aux Channel:

- EDID Support
- MCCS Support
- Remote Command Pass-through Support

EDID and MCCS over DDC/CI are supported by mapping $I^2C$ transaction onto DisplayPort for maintaining the maximum software transparency.

In addition, the AUX CH is expected to be used for an optional content protection feature.

#### *2.5.4.1 DisplayPort Address Mapping for Device Services*

Table 2.42 shows the DisplayPort Address Mapping for Device Services.

**Table 2.42 DisplayPort Address Mapping for Device Services**

| DisplayPort Address | Definition | W/R over Aux.Ch. |
|---|---|---|
| **Reserved Field for DPCP** | | |
| 80000h - 80FFFh | Reserved for DPCP | |
| **Remote Command Pass-through Field** | | |
| 81000h -81FFFh | Reserved for Remote Command Pass-through | |
| **Reserved** | | |
| 82000h - FFFFFh | Reserved | Read all 0's |

#### *2.5.4.2 E-DDC Support through $I^2C$ Mapping*

The Enhanced Display Data Channel (E-DDC) described in "E-DDC Standard Version 1.1 March 24, 2004", allows the display to inform the host about its identity and capability using an $I^2C$ bus. E-DCC enables the communication channel to address a larger set of data than the 128-bytes. E-DDC allows access of up to 32 Kbytes of data based on segment pointer which allows access to multiple blocks of 256 bytes.

Using the $I^2C$ bus transaction mapping described in Section 2.4.4 on p.90, E-DDC transactions can be supported over DisplayPort AUX CH as shown below.

**Example 1: EDID read over Enhanced DDC (128-byte read)**

**Native $I^2C$ transaction**

Start► 0110000|0(i.e., $I^2C$ address=60h)►ACK◄ SegmentPointer7:0► ACK◄ RepeatedStart►
1010000|0(i.e., $I^2C$ address=A0h)►ACK◄ o7:0► RepeatedStart►
1010000|1(i.e., $I^2C$ address = A1h► ACK◄ d0_7:0◄ACK► ... d127_7:0◄ACK► Stop►

**DisplayPort AUX CH transaction**

Request transaction by DisplayPort transmitter

SYNC► 0100|0000 (i.e., I²C write transaction, MOT bit set to 1, ADDR19:16=0000)► 00000000(=ADDR15:8)► 00110000(=ADDR7:0, 7-bit I²C address for E-DCC)► 00000000(i.e., 1 byte write)► SegmentPointer7:0► STOP►

Reply transaction by DisplayPort receiver

SYNC◄ 0000|0000(=ACK)◄ STOP

Request transaction by DisplayPort transmitter

SYNC► 0100|0000 (i.e., I²C write transaction, MOT bit = 1, ADDR19:16=0000)► 01010000(=ADDR15:8)► 01010000 (=ADDR7:0, 7-bit I²C address for EDID)► 00000000(i.e., 1-byte write)► o7:0► STOP►

Reply transaction by DisplayPort receiver

SYNC◄ 0000|0000(=ACK)◄ STOP

Request transaction by DisplayPort transmitter

SYNC► 0101|0000 (i.e., I²C read transaction, MOT bit = 1, ADDR19:16=0000)► 01010000(=ADDR15:8)► 01010000 (=ADDR7:0, -bit I²C address for EDID)► 00001111 (i.e., 16-byte read)► STOP►

….

#### *2.5.4.3 MCCS over DDC/CI Support through I²C Mapping*

The MCCS is a list of commands that comply with the VESA Monitor Control Command Set Standard – Version 2, Revision 1 adopted on May 28th, 2005,, referred to as the MCCS Standard.

Using the I²C bus transaction mapping described in Section 2.4.4 on p.90, "MCCS transactions over DDC/CI" can be supported over DisplayPort AUX CH.

#### *2.5.4.4 Remote Command Pass-through Support*

When both Source and Sink Devices support Remote Command Pass-through as defined in CEA931-B specification, the Source Device shall check the pending command of the Sink Device when it detects that the HPD has toggled and that the cause of the HPD toggle is the pending command of Remote Command Pass-through within 100 ms after the rising edge of HPD signal.

# 3 Physical Layer

## *3.1 Introduction*

The DisplayPort Physical Layer decouples data transmission electrical specifications from the DisplayPort Link Layer, thereby allowing modularity for future link layer specific design enhancement. The physical layer is further sub-divided into logical and electrical functional sub-blocks as shown in Figure 3.1.

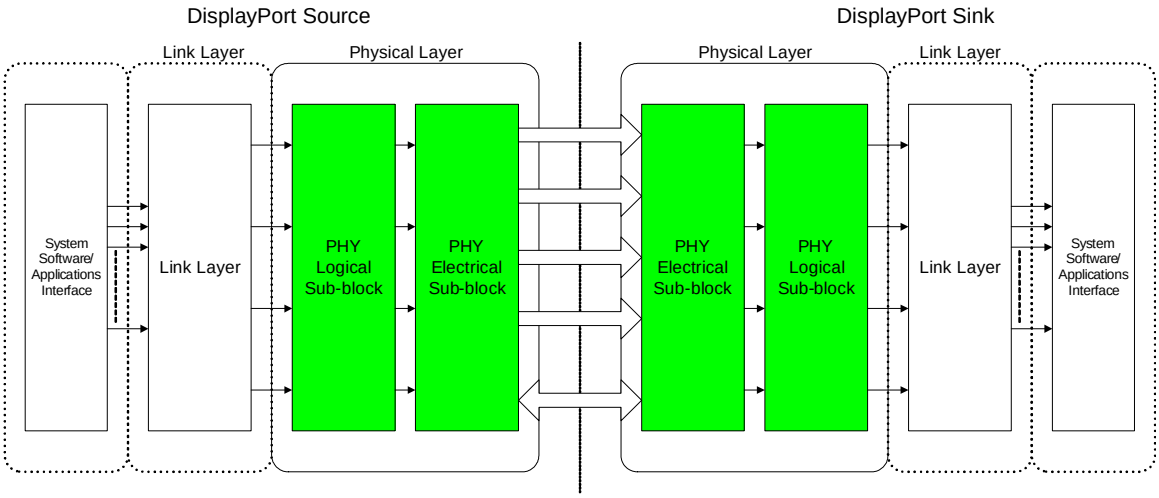



**Figure 3.1 DisplayPort Physical Layer**

### 3.1.1 PHY Functions

This section summarizes the functionalities of the DisplayPort Physical Layer.

#### *3.1.1.1 Hot Plug/Unplug Detection Circuitry*

Physical Layer is responsible both for the detection of Hot Plug/Unplug and the notification to Link Layer.

- Logical Sub-block
  - Notifies of Hot Plug/Unplug event to the upper layer
- Electrical Sub-block
  - Detects Hot Plug/Unplug event

#### *3.1.1.2 AUX Channel Circuitry*

Physical Layer provides for the half-duplex bi-directional AUX Channel for services such as Link Configuration/Maintenance and EDID access.

- Logical Sub-block
  - Generates and detects Start/Stop condition, and locks to the Sync pattern
  - Encoding and decoding of data using Manchester-II coding: DC-balanced and self-clocked
- Electrical Sub-block
  - Consists of single differential pair, both ends of the link equipped with driver and receiver for half-duplex bi-directional operation
  - Driving end
    - Drives doubly-terminated and AC-coupled differential pair in a manner compliant with the AUX Channel Electrical Specification
  - Receiving end
    - Receives the incoming differential signal and extracts data

#### *3.1.1.3 Main Link Circuitry*

Physical Layer provides for the uni-directional Main Link for the transport of isochronous streams and secondary-data packets.

- Logical Sub-block
  - Scrambling and de-scrambling
  - ANSI8B10B encoding/decoding
  - Serialization and de-serialization
  - Link Training and Link Status Monitor
    - Adjusts drive current/pre-emphasis level as needed
  - Link Quality Measurement for testability
- Electrical Sub-block
  - Consists of up to four differential pairs
  - Transmitter

- Drives doubly-terminated and AC-coupled differential pairs in a manner compliant with the Main Link Transmitter Electrical Specification

- Receiver
  - Receives the incoming differential signals and extract data with its link CDR (clock-to-data recovery) circuits

### 3.1.2 Link Layer-PHY Interface Signals

This section summarizes the interface signals between Link Layer and Physical Layer

#### *3.1.2.1 Hot Plug/Unplug Detection*

Hot Plug/Unplug Detection circuitry provides for the Hot Plug/Unplug Status signal to Link Layer.

The de-bouncing timer shall belong to Link Layer, not Physical Layer.

#### *3.1.2.2 AUX Channel*

The interface signal for AUX Channel between Link Layer and Physical Layer shall consist of 8-bit data signal plus 1-bit control signal. The control signal is used to indicate Start and Stop of AUX CH transaction. How to use the 1-bit control signal to indicate Start/Stop conditions is implementation specific and shall not be covered in this specification.

#### *3.1.2.3 Main Link*

The interface signal for Main Link between Link Layer and Physical Layer consists of 8-bit data signal per Main Link lane plus 1-bit control signal. The control signal is used for special symbols such as BS (Blank Start) and BE (Blank End) for framing isochronous data stream. How to use the 1-bit control signal to indicate the usage of special symbols is implementation specific and shall not be covered in this specification.

### 3.1.3 PHY-Media Interface Signals

This section summarizes the interface signals between Physical Layer and the Link Media consisting of PCB (using FR4 material), connector, and cable. (Connector and cable may be absent for certain link configurations such as chip-to-chip connection.)

#### *3.1.3.1 Hot Plug/Unplug Detection*

One signal (HPD, or Hot Plug Detect) is used for this detection. Implementation of HPD is optional for embedded link configuration. At least a “trickle power” must be present both in Source and Sink for Hot Plug event to be detected.

#### *3.1.3.2 AUX Channel*

AUX Channel consists of one differential pair (AUX-CH+ and AUX-CH-). At least a “trickle power” must be present both in Source and Sink for the AUX Channel to be functional.

### *3.1.3.3 Main Link*

Main Link consists of up to four differential pair (Main-Link Lane0+, Main-Link Lane0-, Main-Link Lane1+, Main-Link Lane1- …). Both Source and Sink must be fully powered for the Main Link to be functional.

### *3.1.3.4 Power over Detachable DisplayPort Connector*

DisplayPort connectors for detachable, box-to-box connections have one power pin and one return current pin. The power shall be provided by Source Device only.

The voltage of the power pin shall be in the range of 5- to 12-V. Maximum current drawn from this pin shall be 500 mA. The DisplayPort specification does not specify its usage.

The device that uses this power shall have a power limiting capability that limits the maximum current to 500mA as shown in Table 3.1. The minimum power capacity of the DP_PWR pin shall be 1.0W regardless of the power supply voltage. DisplayPort Device with Sink Function that consumes more than 1.0W of power shall have means of getting power from alternate power source.

**Table 3.1 DP_PWR Specification for Box-to-Box DisplayPort Connection**

| Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|
| Voltage Range | 4.5 | | 13.2 | Volt | 5V - 12V nominal |
| Current Capacity | | | 500 | mA | Connector shall support this maximum current value. |
| Power Capacity | 1.0 | | | Watt | Device with Sink Function consuming more than 1.0W shall get power from other power sources |

When there is Branch Device (for example, DisplayPort-to-Legacy converter or DisplayPort repeater (also known as “cable extender”) getting power from this power pin, there may not be enough power left for powering the receiver of Sink Device. Therefore, it is recommended that a DisplayPort Sink Device have its own power. Even for Branch Device, its operation may fail when more than one Branch Devices are cascaded.

## 3.2 Hot Plug/Unplug Detect Circuitry

The HPD signal is asserted by the DisplayPort Sink whenever the Sink is connected to its main power supply. HPD signal specification is shown in Table 3.2.

**Table 3.2 Hot Plug Detect Signal Specification**

| Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|
| HPD Voltage | 2.25 | | 3.6 | Volt | HPD signal to be driven by Sink Device |
| Hot Plug Detection Threshold | 2.0 | | | Volt | HPD signal to be detected by Source Device |
| Hot Unplug Detection Threshold | | | 0.8 | Volt | |
| IRQ HPD Pulse Width Driven by Sink | 0.5 | | 1.0 | ms | Sink generates a low-going pulse within this range for IRQ (interrupt request) to Source |
| IRQ HPD Pulse Detection Threshold | 2.0 | | | ms | When the pulse width is narrower than this threshold, Source shall read the link/sink status field of DPCD first and take corrective action. When the pulse width is wider than this threshold, it is likely to be actual cable unplug/re-plug event. Upon detecting HPD high, Source shall read link/sink status field, and if link is unstable, read the link/sink capability field of DPCD before initiating Link Training. |

The voltage level of the HPD pin is monitored by Source Device. TTL level shall be used for the detection.

Sink Device may detect the presence of Source Device by monitoring DP_PWR voltage. This monitoring by Sink Device is optional.

## 3.3 AUX Channel

The DisplayPort AUX Channel is a half-duplex, bi-directional channel consisting of one differential pair as shown in Figure 3.2, supporting the bit rate of about 1Mbps, for all the channel lengths. The AUX Channel is doubly terminated with 50Ω termination resistors on both ends, and AC-coupled on the DisplayPort transmitter end. The Manchester-II code is used for the self-clocked transmission of signals as shown below in Figure 3.3.

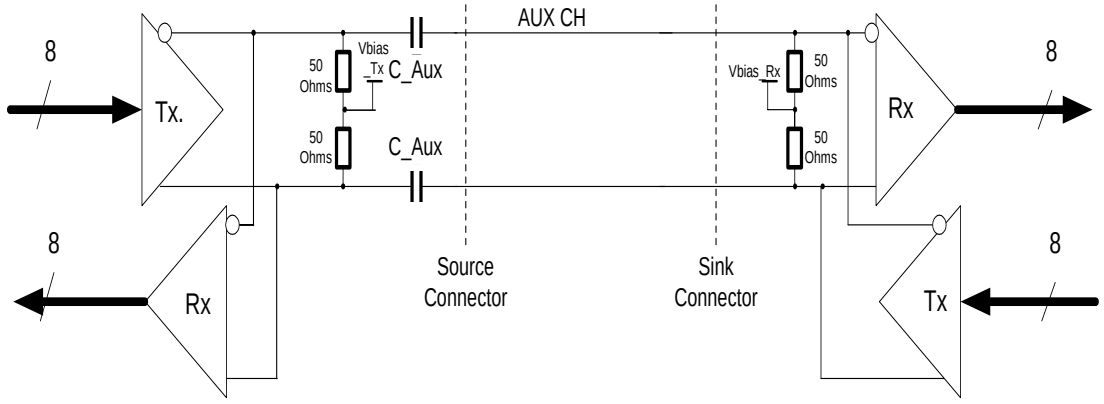



**Figure 3.2 AUX CH Differential Pair**

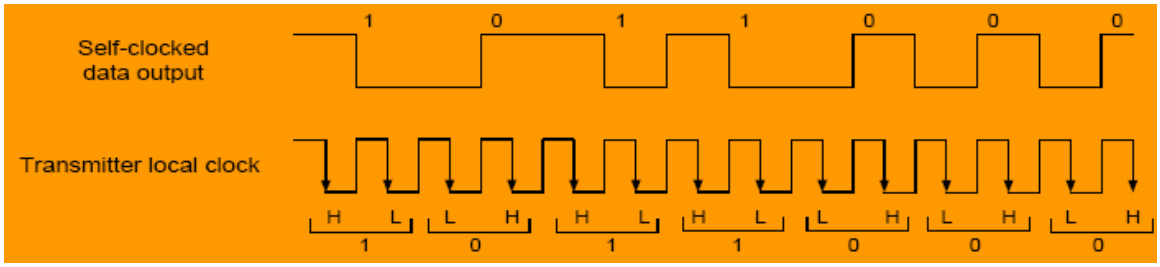



**Figure 3.3 Self-clocking with Manchester II coding**

### 3.3.1 AUX Channel Logical Sub-Block

In-between transactions, AUX Channel is in Electrical Idle state. In the Electrical Idle state, neither device is driving the channel and, thus, both AUX-CH+ and AUX-CH- are parked at the termination voltage.

AUX Channel transactions are initiated by the DisplayPort transmitter which acts as AUX CH requester. The DisplayPort transmitter, which is the driving end for a request transaction, pre-charges AUX-CH+ and AUX-CH- to a common mode voltage. This pre-charge shall be 10 µs or more.

After the pre-charge, the transmitter sends Sync pattern. The Sync pattern shall be as follows:

- Start with 16 consecutive 0's in Manchester II code, which results in transition from L to H in the middle of each bit period
- End with AUX-CH+ driven to H for 2-bit period (which is 2 us when the bit rate is 1Mbps) and L for 2-bit period, which is illegal in Manchester II code. (AUX-CH- shall be driven to the opposite polarity.)

The receiving end, which is the DisplayPort receiver for the request transaction, shall lock to this Sync pattern.

Following the Sync pattern, the driving end shall send data according to the AUX CH syntax as described Section 2.4 starting from p.87. When it has finished sending data, the driving node shall assert STOP condition. The STOP condition shall be as follows:

- Drives AUX-CH+ to H and AUX-CH- to L for 2-bit period, then AUX-CH+ to L and AUX-CH- to H for 2-bit period, which is an illegal sequence for Manchester II
- Releases AUX CH right after STOP condition

The DisplayPort receiver, AUX CH replier, replies to this request transaction. The DisplayPort receiver, now acting as a driving end, shall let the bus park for at least 10ns, pre-charges the bus to the common mode voltage for at least 10us, and initiates the reply transaction. The Sync pattern and the STOP condition are the same whether it is a request transaction or a reply transaction.

### 3.3.2 AUX Channel Electrical Sub-Block

Table 3.3 below shows the electrical specification of the DisplayPort AUX Channel.

**Table 3.3 DisplayPort AUX Channel Electrical Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | AUX Unit Interval | 0.4 | 0.5 | 0.6 | μs | Results in the bit rate of 1Mbps including the overhead of ManchesterII coding. |
| $T_{AUX-BUS-PRECHARGE}$ | AUX CH bus pre-charge time | 10 | | 50 | μs | Period for which the driving device pre-charges the AUX CH bus to a common voltage |
| $T_{AUX-BUS-PARK}$ | AUX CH bus park time | 10 | | | ns | Period after AUX CH STOP condition for which the bus is parked |
| $V_{AUX-DIFFp-p}$ | AUX Peak-to-peak Voltage | 0.19 | | 1.26 | V | $V_{TXAUX-DIFFp-p} = 2*\|V_{TX-AUXP} - V_{TX-AUXM}\|$ |
| $V_{AUX-DC-CM}$ | AUX DC Common Mode Voltage | 0 | | VDD | V | Common mode voltage is equal to Vbias_Tx (or Vbias_Rx) voltage shown in Figure 3.2. VDD is the power supply voltage of AUX CH driver/receiver and 3.6V maximum. |
| $I_{AUX\_SHORT}$ | AUX Short Circuit Current Limit | | | 90 | mA | Total drive current of the transmitter when it is shorted to its ground. |
| $R_{AUX-DIFF}$ | Differential AUX TX termination resistance | 90 | 100 | 110 | Ω | AUX CH is doubly terminated, just as the Main Link |
| $R_{AUX-SE}$ | Single-ended AUX termination resistance | 45 | 50 | 55 | Ω | |
| $C_{AUX}$ | AUX AC Coupling Capacitor | 75 | | 200 | nF | AUX CH AC coupling capacitor placed on the DisplayPort Source Device side |

#### *3.3.2.1 AC Coupling*

The DisplayPort AUX Channel shall be AC-coupled. The minimum and maximum values for the capacitance are specified in Table 3.3. The requirement for the inclusion of AC coupling capacitors on the interconnect media is specified at the DisplayPort transmitter. Inclusion of the AC coupling capacitors at the DisplayPort receiver is optional.

#### *3.3.2.2 Termination*

The DisplayPort AUX Channel is required to meet the termination impedance as specified in Table 3.3, any time the link is active.

### *3.3.2.3 DC Common Mode Voltage*

Due to the bi-directional nature of the DisplayPort AUX Channel, the allowable common mode voltage of AUX CH has to be limited as to avoid excessive switch-over spikes as defined in Table 3.3.

### *3.3.2.4 Short Circuit Requirements*

The driver and receiver circuits of AUX CH block must survive the worst-case short-circuit current of 90mA (3.6V over 40Ω).

### *3.3.2.5 Differential voltage/timing (EYE) diagram*

The EYE diagram is used to measure compliance of the signal into the test load for the specified number of UI's. It must be noted that while the EYE is a compliance measurement, it does not guarantee that the jitter specification has been met. Jitter requirements listed elsewhere in this specification must be met in addition to the eye diagram to comply with this specification. Down-spreading of the link clock should be disabled for the capture of data to be used with the EYE masks.

The masks in Figure 3.4 show two polygons. The dashed-outer polygons represent the 5UI mask and the solid-inner polygons represent the 250UI eye mask. Table 3.4 contains the values to be used for the vertices of the mask.

The diagram may be created using multiple samples, but each sample must be of the specified capture length and normalized to the average UI of the sample interval.

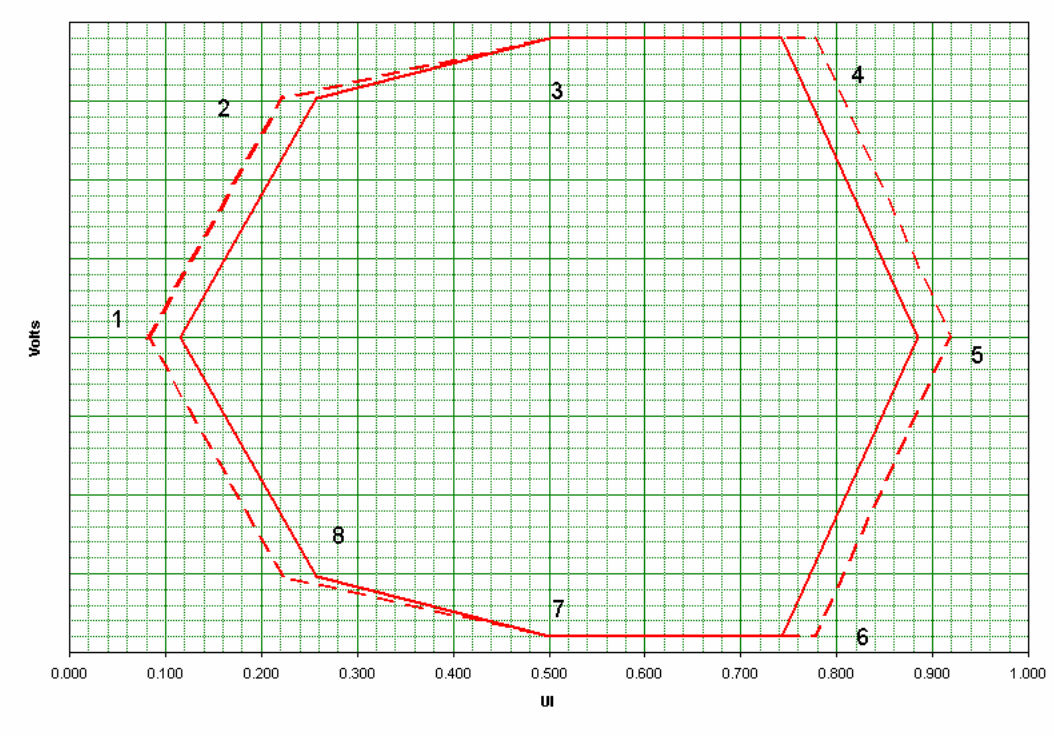



**Figure 3.4 AUX CH EYE Mask**

**Table 3.4 Mask Vertices Table for AUX CH at Chip Pins of Receiving End**

| Point | Time: 5 UI | Time: 250 UI | Minimum voltage value at 8 Vertices (Volts) |
|---|---|---|---|
| 1 | 0.010 | 0.014 | 0.000 |
| 2 | 0.020 | 0.024 | 0.065 |
| 3 | 0.500 | 0.500 | 0.085 |
| 4 | 0.980 | 0.976 | 0.085 |
| 5 | 0.990 | 0.986 | 0.000 |
| 6 | 0.980 | 0.976 | -0.085 |
| 7 | 0.500 | 0.500 | -0.085 |
| 8 | 0.020 | 0.024 | -0.065 |

## *3.4 Main Link*

This section describes the functionalities of the DisplayPort Main Link Physical layer.

### 3.4.1 Main Link Logic Sub-block

The Logical Sub-block of DisplayPort Main Link Physical Layer performs the following functionalities:

- Scrambling and de-scrambling
- ANSI 8B/10B encoding/decoding
- Serialization and de-serialization
- Link Training and Link Status Monitor
  - Drive current/pre-emphasis level control as needed
- Link Quality Measurement (Testability)

#### *3.4.1.1 Scrambling*

Scrambling of Main Link data is performed for EMI reduction prior to ANSI 8B/10B encoding on the transmitter. Likewise, de-scrambling of data symbols is performed subsequent to ANSI 8B/10B decoding at the receiver. Utilization of scrambling should result in approximately 7dB in peak spectrum reduction.

Each of Main Link lanes is scrambled and de-scrambled independently, each with a 16-bit LFSR as follows:

- $G(X) = X16 + X5 + X4 + X3 + 1$

The Physical Layer of the Source Device shall replace every $512^{th}$ BS symbol with SR symbol. The SR symbol is used to reset the LFSR to FFFFh.

The data scrambling rules shall be as follows:

- Special symbols (K-codes) are not scrambled. The LFSR does not advance for the K-codes.
- Data symbols, including "fill data" are scrambled

Note that the scrambling must be disabled during Link Training and Recovered Link Clock Quality Measurement.

An example of the scrambler/de-scrambler is shown in the next section.

#### 3.4.1.1.1 VHDL Code Fragment of Scrambler/De-scrambler (INFORMATIVE)

The following VHDL example shows an HDL implementation of the Scrambler/De-scrambler. The 8-bit Scrambler/De-Scrambler are used for each lane of Main Link.

```
------------------------------------------------------------------
8-bit Scrambler/De-Scrambler
------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;

entity scrambler_byte is
  port (
    iCLK          : in std_logic;
    iRESET        : in std_logic;
    iEN           : in std_logic;
    iDATA         : in std_logic_vector(7 downto 0);
    iBS_VBID_CHAR : in std_logic;        -- Char to reset LFSR
    iTS           : in std_logic;        -- K-Code Timing Sequence
    oDATA         : out std_logic_vector(7 downto 0)
  );
end scrambler_byte;

architecture RTL of scrambler_byte is

signal lfsr : std_logic_vector(15 downto 0);

begin

  -- Data scrambling
  process (iCLK, iRESET)
  begin
    if (iRESET = '1') then
      oDATA <= (others => '0');
    elsif (iCLK'event and iCLK = '1') then
```

```
    if (iEN = '1') then
      if (iBS_VBID_CHAR = '1' or iTS = '1') then
        -- bypass scrambler
        oDATA <= iDATA;
      elsif (iBS_VBID_CHAR = '0' and iTS = '0') then

        oDATA(0) <= iDATA(0) xor lfsr(15);
        oDATA(1) <= iDATA(1) xor lfsr(14);
        oDATA(2) <= iDATA(2) xor lfsr(13);
        oDATA(3) <= iDATA(3) xor lfsr(12);
        oDATA(4) <= iDATA(4) xor lfsr(11);
        oDATA(5) <= iDATA(5) xor lfsr(10);
        oDATA(6) <= iDATA(6) xor lfsr(9);
        oDATA(7) <= iDATA(7) xor lfsr(8);
      else
        oDATA <= iDATA;
      end if;
    else
      oDATA <= iDATA;
    end if;
  end if;
end process;

-- lfsr generation
process (iCLK, iRESET)
begin
  if (iRESET = '1') then
    lfsr <= (others => '1');
  elsif (iCLK'event and iCLK = '1') then
    if (iBS_VBID_CHAR = '1') then
      -- reset lfsr
      lfsr <= (others => '1');
    elsif (iTS = '1') then
      -- don't advance lfsr
```

```
        lfsr <= lfsr;
      else
-- This is for X^16 + X^15 + X^13 + X^4 + 1 polynomial in parallel,
-- which advances lfsr by 8 bits
        lfsr(0)  <= lfsr(15) xor lfsr(12) xor lfsr(10) xor lfsr(9) xor lfsr(8);
        lfsr(1)  <= lfsr(13) xor lfsr(11) xor lfsr(10) xor lfsr(9);
        lfsr(2)  <= lfsr(14) xor lfsr(12) xor lfsr(11) xor lfsr(10);
        lfsr(3)  <= lfsr(15) xor lfsr(13) xor lfsr(12) xor lfsr(11);
        lfsr(4)  <= lfsr(15) xor lfsr(14) xor lfsr(13) xor lfsr(10) xor lfsr(9) xor lfsr(8);
        lfsr(5)  <= lfsr(15) xor lfsr(14) xor lfsr(11) xor lfsr(10) xor lfsr(9);
        lfsr(6)  <= lfsr(15) xor lfsr(12) xor lfsr(11) xor lfsr(10);
        lfsr(7)  <= lfsr(13) xor lfsr(12) xor lfsr(11);
        lfsr(8)  <= lfsr(14) xor lfsr(13) xor lfsr(12) xor lfsr(0);
        lfsr(9)  <= lfsr(15) xor lfsr(14) xor lfsr(13) xor lfsr(1);
        lfsr(10) <= lfsr(15) xor lfsr(14) xor lfsr(2);
        lfsr(11) <= lfsr(15) xor lfsr(3);
        lfsr(12) <= lfsr(4);
        lfsr(13) <= lfsr(15) xor lfsr(12) xor lfsr(10) xor lfsr(9) xor lfsr(8) xor lfsr(5);
        lfsr(14) <= lfsr(13) xor lfsr(11) xor lfsr(10) xor lfsr(9) xor lfsr(6);
        lfsr(15) <= lfsr(15) xor lfsr(14) xor lfsr(11) xor lfsr(9) xor lfsr(8) xor lfsr(7);

-- This is for X^16 + X^15 + X^13 + X^4 + 1 polynomial series type LFSR, which not used
        --lfsr(0)  <= lfsr(15);
        --lfsr(1)  <= lfsr(0);
        --lfsr(2)  <= lfsr(1);
        --lfsr(3)  <= lfsr(2);
        --lfsr(4)  <= lfsr(15) xor lfsr(3);
        --lfsr(5)  <= lfsr(4);
        --lfsr(6)  <= lfsr(5);
        --lfsr(7)  <= lfsr(6);
        --lfsr(8)  <= lfsr(7);
        --lfsr(9)  <= lfsr(8);
        --lfsr(10) <= lfsr(9);
        --lfsr(11) <= lfsr(10);
```

```
      --lfsr(12) <= lfsr(11);
      --lfsr(13) <= lfsr(15) xor lfsr(12);
      --lfsr(14) <= lfsr(13);
      --lfsr(15) <= lfsr(15) xor lfsr(14);
    end if;
  end if;
 end process;


end RTL;
```

---------- End of example ----------

#### *3.4.1.2 Symbol Coding and Serialization/De-serialization*

The DisplayPort interface uses the ANSI standard 8B/10B[1] as its channel coding scheme to provide symbol-level DC balancing. It also provides high transition density for link clock phase tracking at the receiver. Using this scheme, 8-bit data characters are treated as three bits and five bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the Special Symbols included in the 8B/10B transmission code. These code groups are concatenated to form a 10-bit symbol. As shown in Figure 3.5, ABCDE maps to abcdei and FGH maps to fghj.

After coding, the ANS 8B/10B symbols are serialized so that the least significant bit (LSB) is transported first, and the most significant bit (MSB) last.

[1] The 8B/10B coding scheme is as defined in ANSI X3.230-1994, clause 11 (and also 802.3z, 36.2.4).

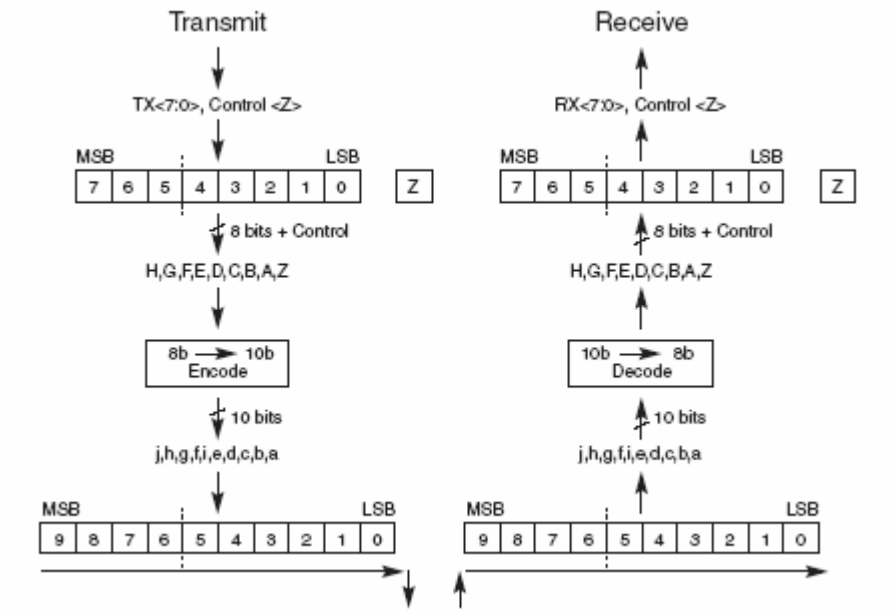



**Figure 3.5 Character to symbol mapping**

#### 3.4.1.2.1 ANSI 8B/10B Special Characters used for DisplayPort Control Symbols

In DisplayPort Specification Ver.1.0, seven control symbols are defined in the Link Layer (refer to Section 2.2.1.1 on p.35. Table 3.5 shows which ANSI 8B/10B special characters are used for those control symbols. Unused special characters are reserved for future use and shall not be used by DisplayPort Ver.1.0-compliant link.

**Table 3.5 ANSI 8B/10B Special Characters for DisplayPort Ver.1.0 Control Symbols**

| Special Character | Symbol | Name |
|---|---|---|
| K28.5 | BS | Blank Start |
| K27.7 | BE | Blank End |
| K28.2 | SS | Secondary-data Start |
| K29.7 | SE | Secondary-data End |
| K30.7 | FS | Fill Start |
| K23.7 | FE | Fill End |
| K28.0 | SR | Scrambler Reset |
| K28.1 | CPBS | Content Protection BS |
| K28.3 | CPSR | Content Protection SR |
| K28.4, K28.6, K28.7 | Reserved in DisplayPort Ver.1.0. | |

**Note1**: Refer to Section 2.2.1 starting from p.33 for definitions of these control symbols.
**Note2**: As for CPBS and CPSR, refer to APPENDIX 1 on p.204.

### *3.4.1.3 Link Training*

For an open, box-to-box connection, DisplayPort Source Device configures the link through link training sequence. For a closed, embedded connection DisplayPort transmitter and receiver may be set to pre-calibrated parameters without going through the full link training sequence. In this mode, DisplayPort Source Device may start a normal operation following the transmission of Clock Recovery Pattern (as described in detailed in the following sub-section) with pre-calibrated drive current and pre-emphasis level, as shown with a dotted arrow in Figure 2.33 on p.108.

Link training consists of two distinct tasks which must be completed successfully in sequence in order to establish the link. These are:

- Clock Recovery: Locks the receiver CR (clock recovery) PLL to the repetition of D10.2 data symbols. This stage of Link Training determines the drive strength for the link.
- Channel Equalization/Symbol-Lock/Inter-lane Alignment: Optimizes the transmitter equalizer (also known as pre-emphasis). Receiver's equalizer (optional) may also be optimized. When successful, the Symbol-Lock and Inter-lane alignment shall be achieved by the end of this sequence.

The training sequence is initiated by the Link Policy Maker in the Source Device upon detecting HPD event. When Source Device detects a HPD low-going pulse that exceeds 2 ms in width, Link Policy Maker shall read the link capability field of DPCD via AUX CH. Link Policy Maker shall, then, determine the link configuration based on the capability of DisplayPort Receiver and its own needs, write the configuration parameter to the link configuration field of DPCD, and start the Link Training by writing to 01h to TRAINING_PATTERN_SET byte of DPCD (DisplayPort Configuration Data) of DisplayPort receiver via Aux Ch while instructing its transmitter PHY logic sub-layer to start transmitting training patterns.

Link Policy Maker of Source Device may choose any link count and link rate as long as they do not exceed the capabilities of DisplayPort Receiver. Link Training is expected to be completed within 10 ms after Link Policy Maker of Source Device reads the link capability of DisplayPort Receiver. Table 3.6 shows the Link Training symbol patterns.

**Table 3.6 Symbol Patterns of Link Training**

| Pattern Number | Purpose | Name |
|---|---|---|
| 1 | For locking Clock Recovery Circuit of DisplayPort receiver | Repetition of D10.2 characters |
| 2 | For optimizing equalization, determining symbol boundary, and achieving inter-lane alignment | K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2 |

As for complete DisplayPort address mapping and definition for DPCD, refer to the DPCD Address Mapping Table (Table 2.41 starting from 97).

#### 3.4.1.3.1 Clock-Recovery (CR) Sequence

Link training begins with the Clock-Recovery sequence. The link symbols transmitted in this sequence are a repetition of D10.2 data symbols with scrambling disabled. In this sequence, the transmitter shall disable pre-emphasis, and start with the minimum differential voltage swing of 0.4 Vdiff_pp, corresponding to the drive current of 8mA. (The transmitter may start with non-minimum differential voltage swing and with pre-emphasis if the optimal setting is already known, for example, as is the case in embedded application.) The transmitter shall wait for 100 μs before reading the LANEx_CR_DONE bits of DPCD which are set by the receiver.

Once it achieves the CR lock, the receiver shall set the LANEx_CR_DONE bit for each of (up to) 4 lanes in the DPCD. Otherwise, the receiver shall keep LANEx_CR_DONE bits cleared and request for an increase of differential voltage swing by updating the value in ADJUST_REQUEST_LANEx_x bytes. If the receiver keeps the same value in ADJUST_REQUEST_LANEx_x bytes while LANEx_CR_DONE bits remain unset, the transmitter shall loop 4 times with the same voltage swing. On the 5th time, the transmitter shall down-shift to the lower bit rate and shall repeat the CR-lock training sequence.

Unless all the LANEx_CR_DONE bits are set, the transmitter shall read the ADJUST_REQUEST_LANEx_x, increase the drive current according to the request, and update the TRAINING_LANEx_SET bytes to match the new drive current setting.

The transmitter shall support differential voltage swings of 0.4-/0.6-/0.8-Vdiff_pp, which correspond to drive current of 8-/12-/16-mA, respectively (refer to Section 3.4.2.5 on p. 139).

If the maximum differential voltage swing (0.8Vdiff_pp) fails to realize the CR lock, the transmitter shall down-shift to the lower bit rate (as indicated to the receiver by AUX CH write to LINK_BW_SET byte of DPCD), and repeat the bit-lock training sequence.

Once it reads CR_DONE_LANEx bits set for all lanes, the Link Policy Maker of the transmitter shall move on to the next stage, namely, Channel Equalization.

If any one of CR_DONE_LANEx remains 0 even at a reduced bit rate after all the drive current values have been tried, the transmitter shall end the training (by clearing TRAINING_PATTERN_SET byte to 00h in DPCD) without establishing the link.

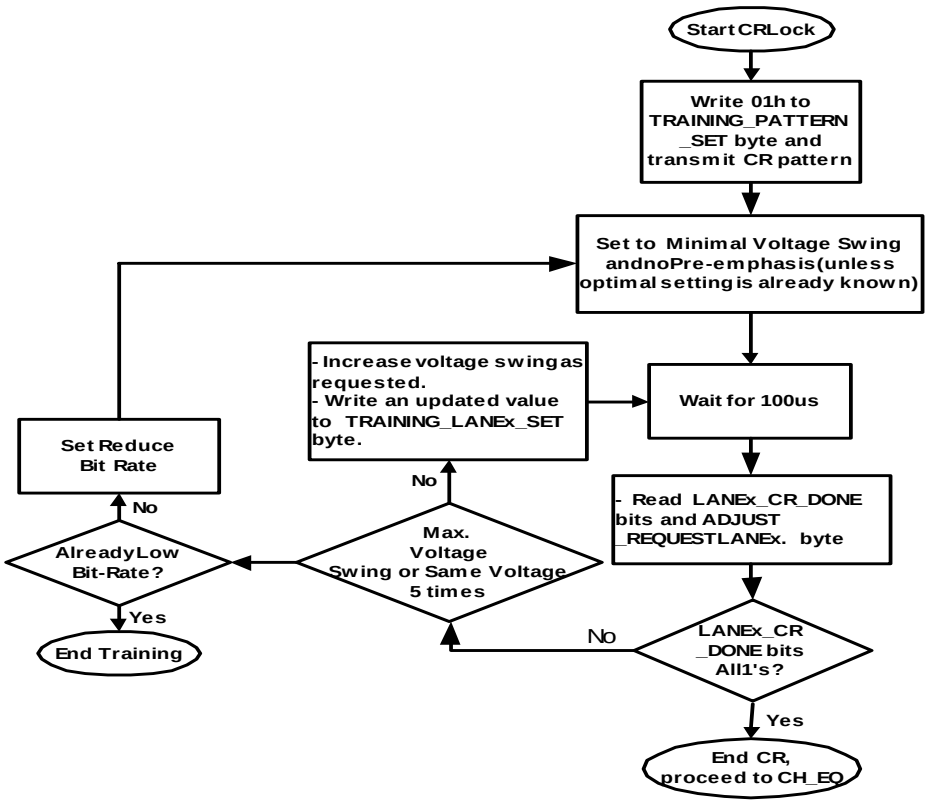



**Figure 3.6 Clock Recovery Sequence of Link Training**

#### 3.4.1.3.2 Channel Equalization (EQ) Sequence

The Channel Equalization sequence starts with the differential voltage swing (Vdiff) set in the Clock Recovery sequence, with pre-emphasis of the transmitter and equalizer of the receiver (optional) both disabled.

In the Channel Equalization (EQ) sequence, the transmitter writes 02h to TRAINING_PATTERN_SET byte of DPCD, and transmits the following ten-symbol pattern repetitively, with scrambling disabled.

- K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2

The transmitter shall insert two-link-symbol inter-lane skew between adjacent lanes as shown in Figure 2.15 on p.58.

The receiver shall use the recognition of this training pattern to decide whether the channel equalization is successful or not. How to measure the equalization result is implementation specific.

The transmitter shall support the pre-emphasis levels of 0-dB (no pre-emphasis), +3.5dB (1.5x), and +6dB (2x) as long as the pre-emphasized differential voltage swing (Vdiff_pre in Figure 3.10 on page 140) does not exceed 1.2V. Support of +9.5dB (3x) is optional. For example, when the differential voltage swing is set to 0.8V_diff_pp in the CR sequence, the maximum pre-emphasis level is limited to +3.5dB (Refer to Section 3.4.2.5 on p.139).

The receiver shall indicate the success by setting LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCKED, and INTERLANE_ALIGN_DONE bits in LANEx_x_STATUS/LANE_ALIGNED_STATUS_UPDATED bytes.

The transmitter shall read those bytes and ADJUST_REQUEST_LANEx_x bytes. Unless all those status bits are 1, the transmitter shall then adjust the pre-emphasis level according to the request by the receiver, and writes the new setting to TRAINING_LANEx_SET bytes.

The receiver with its own equalizer (optional) may adjust its equalizer setting(s) in each of the EQ training loop (as shown as the dotted-box in Figure 3.7).

It is recommended that the receiver not set LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK_DONE, and INTERLANE_ALIGN_DONE bits right after the successful reception of training patterns. Rather, the receiver should either increase its own equalization level or request for a stronger pre-emphasis. When such action results in loss of successful reception, the receiver shall restore or request for the last setting. The purpose of this methodology is to ensure maximum operating margin.

The minimum loop count in this sequence is 1, while the maximum loop count in this sequence (refer to Figure 3.7) shall be 5.

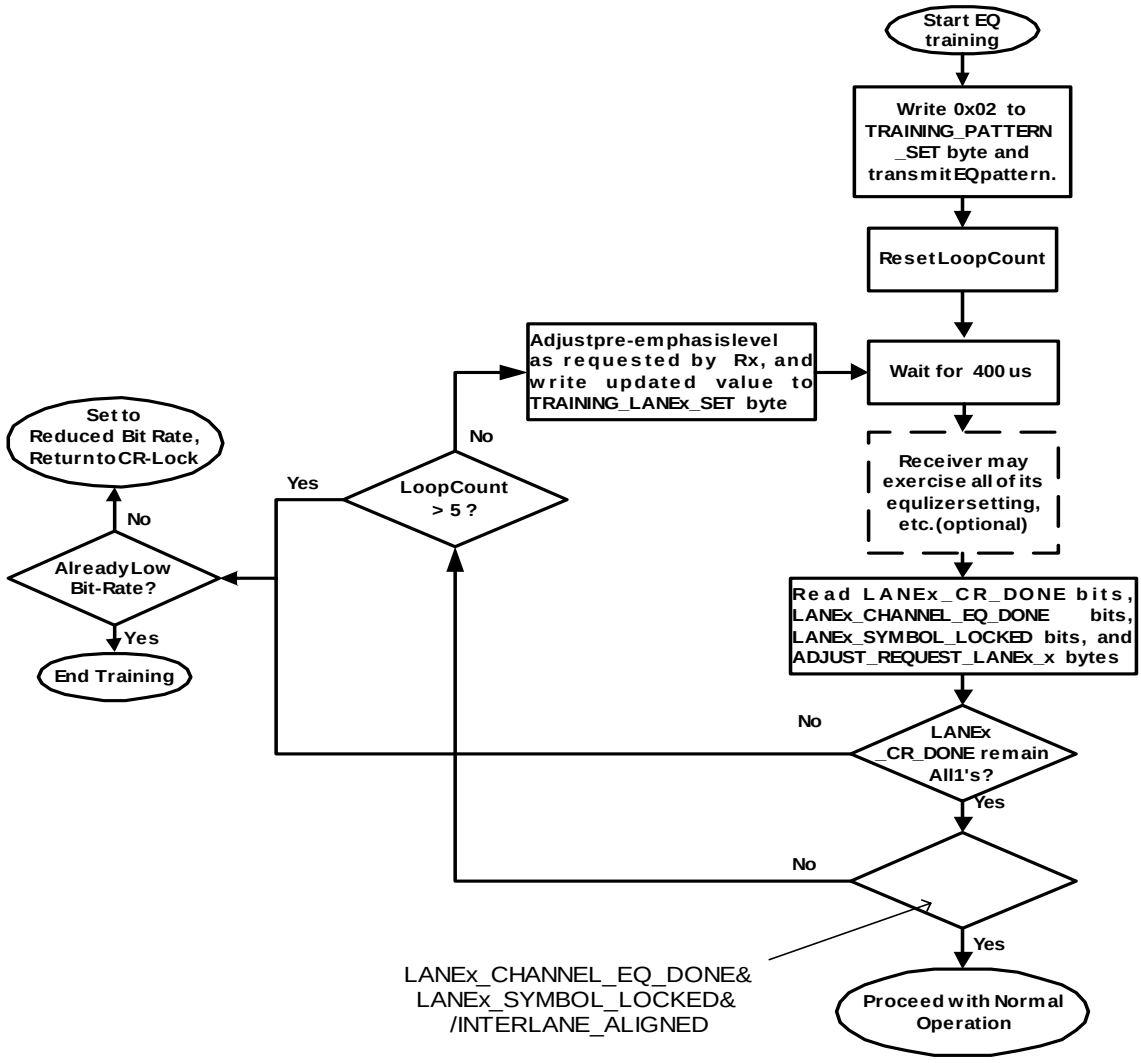



**Figure 3.7 Channel Equalization Sequence of Link Training**

Upon verifying that Channel Equalization/Symbol-Lock/Inter-lane Alignment are all done, the transmitter shall write 00h to TRAINING_PATTERN_SET byte to indicate the end of training, and starts transmission of stream data.

If Clock Recovery circuit loses lock during the Channel Equalization sequence, the receiver shall clear the CR_DONE_LANEx bit. If it is in the high bit-rate mode, the transmitter then shall reduce the bit-rate and return to CR training sequence. If it is already in the reduced bit-rate mode, then the transmitter shall end the training by writing 00h to TRAINING_PATTERN_SET byte without establishing the link.

#### *3.4.1.4 Link Maintenance*

The link status bits may be cleared by the receiver upon loss of either clock recovery lock, symbol lock, or inter-alignment lock. The transmitter shall check the link status whenever it detects low-going IRQ HPD pulse during normal operation (as specified in Section Figure 2.33 on p.108), and perform re-training of the link as needed.

#### *3.4.1.5 Link Quality Measurement (Testability)*

The DisplayPort transmitter shall be able to transmit test patterns for link quality measurement purpose as indicated in Section 2.5.3.5 on p.108.

The DisplayPort receiver shall support for the following:

- **Recovered Link Clock Quality Measurement:** Outputs the recovered link clock from a test pad when the DisplayPort Source Device writes to RECOVERED_CLOCK_OUT_EN bit of TRAINING_PATTERN_SET byte of DPCD. The output clock frequency shall be 1/40 of the link clock frequency. The purpose of this test output is to enable a simple EYE test for jitter measurements with minimal equipment for embedded applications using the recovered clock from the CDR circuits in the receiver. This output is not intended to be used for compliance purposes; such testing is specified in the DisplayPort compliance document. This test output shall support a minimum of 10 pF of parasitic capacitance including that of the test probe. The test output shall add no more than 11ps peak-to-peak jitter at a high bit rate and 18 ps peak-to-peak jitter at a reduced bit rate accumulated for a period of 250UI to facilitate 3% measurement accuracy (+/-1.5%); for example, if a single-ended output pad is desired, the test pad would need a minimum slew rate of 1.82V/ns into the maximum expected capacitive load and can have no more than 20mVp-p of total power supply noise. If the same pad can support 3.64V/ns then 40mVp-p power supply noise can be tolerated.
- **Link Symbol Error Rate Measurement:** Counts the number of unscrambled data that is not 00h when the DisplayPort Source Device writes 08h to TRAINING_PATTERN_SET byte, and stores that count in SYMBOL_ERROR_COUNT_LANEx bytes of DPCD (refer to Table 2.41 starting on 97). Link quality can be estimated using the procedure listed in Section 2.5.3.5 on p.108.

### 3.4.2 Main Link Electrical Sub-Block

The electrical sub-block of a DisplayPort Main Link consists of up to four differential pairs. The DisplayPort Transmitter drives doubly-terminated and AC-coupled differential pairs as shown in Figure 3.8 in a manner compliant with the Main Link Transmitter Electrical Specification. The DisplayPort Receiver receives the incoming differential signals and extracts data with its link CDR (clock-and-data recovery) circuits.

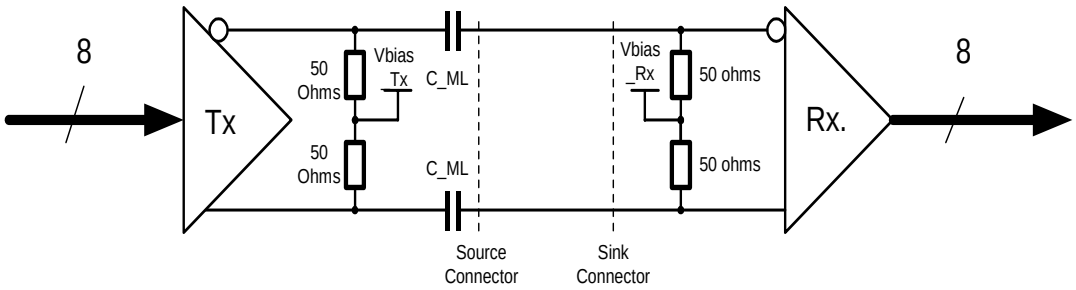



**Figure 3.8 Main Link Differential Pair**

#### *3.4.2.1 Definition of Differential Voltage*

A differential signal is defined by taking the voltage difference between two conductors. In this specification, a differential signal or differential pair is comprised of a voltage on a positive conductor, $V_{D+}$, and a negative conductor, $V_{D-}$. The differential voltage ($V_{DIFF}$) is defined as the difference of the positive conductor voltage and the negative conductor voltage ($V_{DIFF} = V_{D+} - V_{D-}$) as shown in Figure 3.9. The Common Mode Voltage ($V_{CM}$) is defined as the average or mean voltage present on the same differential pair ($V_{CM} = [V_{D+} + V_{D-}]/2$).

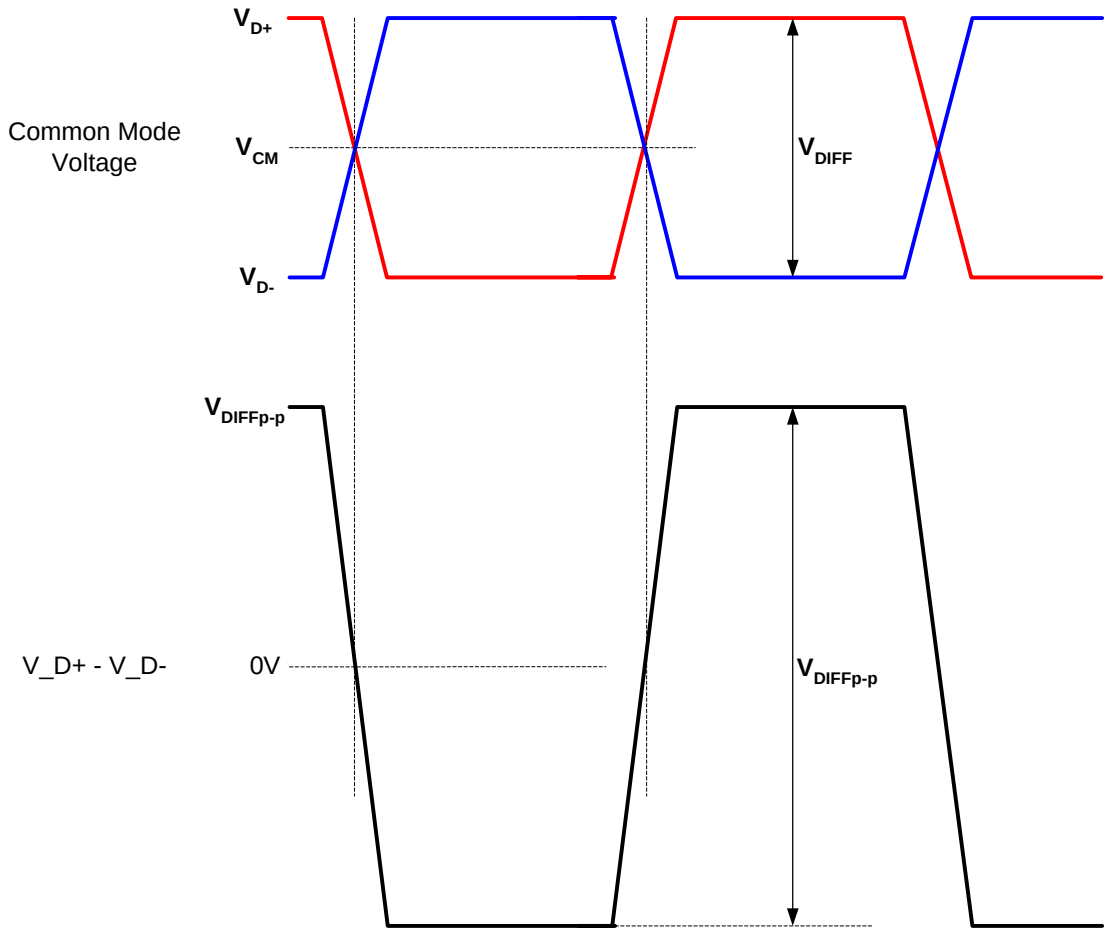



**Figure 3.9 Definition of Differential Voltage and Differential Voltage Peak-to-Peak**

This document's electrical specifications often refer to peak-to-peak measurements or peak measurements, which are defined by the following equations:

Symmetrical Differential Swing

$V_{DIFFp\text{-}p} = (2*\max|V_{D+} - V_{D-}|)$

$V_{DIFFp} = (\max|V_{D+} - V_{D-}|)$

Asymmetrical Differential Swing

$V_{DIFFp\text{-}p} = (\max|V_{D+} - V_{D-}|\ \{V_{D+} > V_{D-}\} + \max|V_{D+} - V_{D-}|\ \{V_{D+} < V_{D-}\})$

$V_{DIFFp} = (\max|V_{D+} - V_{D-}|\ \{V_{D+} > V_{D-}\})$ or $(\max|V_{D+} - V_{D-}|\ \{V_{D+} < V_{D-}\})$ whichever is greater

Common-Mode Voltage

$V_{CMp} = (\max|V_{D+} + V_{D-}|/2)$

The definition equations only produce a single number (the number in the spec tables) and are not suitable for plotting a waveform.

Table 3.7 and Table 3.8 show the Main Link Transmitter Electrical Specifications and Main Link Receiver Electrical Specifications, respectively.

**Table 3.7 DisplayPort Main Link Transmitter (Main TX) Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI_High_Rate | Unit Interval for High Bit Rate (2.7Gbps/lane) | 368 | 370 | 372 | ps | UI does not account for down-spread dictated variations. |
| UI_Low_Rate | Unit Interval for Reduced Bit Rate (1.62Gbps/lane) | 614 | 617 | 620 | ps | |
| Down_Spread_Amplitude | Link clock down spreading | 0 | | 0.5 | % | |
| Down_Spread_Frequency | Link clock down-spreading frequency | 30 | | 33 | kHz | |
| $V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$ | Differential Peak-to-peak Output Voltage Level 1 | 0.36 | 0.4 | 0.44 | V | Refer to 0 and Figure 3.10 for definition of differential voltage. |
| $V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$ | Differential Peak-to-peak Output Voltage Level 2 | 0.54 | 0.6 | 0.66 | V | |
| $V_{TX\text{-}DIFFp\text{-}p\text{-}Level3}$ | Differential Peak-to-peak Output Voltage Level 3 | 0.72 | 0.8 | 0.88 | V | |
| $V_{TX\text{-}DIFFp\text{-}p\text{-}Level4}$ | Differential Peak-to-peak Output Voltage Level 4 | 1.08 | 1.2 | 1.32 | V | |
| $V_{TX\text{-}PREEMP\text{-}RATIO}$ | No Pre-emphasis | 0.0 | 0.0 | 0.0 | dB | Refer to 0 and Figure 3.10 for definition of differential voltage. Support of no pre-emphasis, 3.5- and 6.0-dB pre-emphasis mandatory. 9.5-dB level optional. |
| | 3.5 dB Pre-emphasis Level | 2.9 | 3.5 | 4.1 | dB | |
| | 6.0 dB Pre-emphasis Level | 5.1 | 6.0 | 6.9 | dB | |
| | 9.5 dB Pre-emphasis Level | 8.3 | 9.5 | 10.7 | dB | |
| Tx Horizontal Eye Specification for High Bit Rate | | | | | | |
| $T_{TX\text{-}EYE\_CHIP\_High\_Rate}$ | Minimum TX Eye Width at Tx package pins | 0.74 | | | UI | |
| $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\_CHIP\_\_High\_Rate}$ | Maximum time between the jitter median and maximum deviation from the median at Tx package pins | | | 0.13 | UI | |
| Tx Horizontal Eye Specification for Reduced Bit Rate | | | | | | |
| $T_{TX\text{-}EYE\_CHIP\_Low\_Rate}$ | Minimum TX Eye Width | 0.84 | | | UI | |
| $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\ CHIP\ Low\_Rate}$ | Maximum time between the jitter median and maximum deviation from the median at Tx package pins | | | 0.08 | UI | |
| $T_{TX\text{-}RISE\_CHIP}$, $T_{TX\text{-}FALL\_CHIP}$ | D+/D- TX Output Rise/Fall Time at Tx package pins | | | 110 | ps | At 20-to-80 |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{TX-DC-CM}$ | TX DC Common Mode Voltage | 0 | | VDD | V | Common mode voltage is equal to Vbias_Tx voltage shown in Figure 3.8. VDD is the output driver power supply voltage and 3.6V maximum. |
| $I_{TX-SHORT}$ | TX Short Circuit Current Limit | | | 90 | mA | Total drive current of the transmitter when it is shorted to its ground. |
| $RL_{TX-DIFF}$ | Differential Return Loss at 0.675GHz | | | 12 | dB | Straight loss line between 0.675 GHz and 1.35GHz |
| | Differential Return Loss at 1.35GHz | | | 9 | dB | |
| $R_{TX-SE}$ | Single-ended TX resistance | 45 | 50 | 55 | Ω | |
| $L_{TX-SKEW-INTER\_CHIP}$ | Lane-to-Lane Output Skew at Tx package pins | | | 150 | ps | |
| $L_{TX-SKEW-INTRA\_CHIP}$ | Lane Intra-pair Output Skew at Tx package pins | | | 20 | ps | |
| $C_{TX}$ | AC Coupling Capacitor | 75 | | 200 | nF | All DisplayPort Main Link lanes as well as AUX CH shall be AC coupled. AC coupling capacitors shall be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional. |
| $F_{TX-REJECTION-BW}$ | Clock Jitter Rejection Bandwidth | | | 4 | MHz | |

**Table 3.8 DisplayPort Main Link Receiver (Main RX) Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI_High_Rate | Unit Interval for High Bit Rate (2.7Gbps/lane) | 367 | 370 | 373 | ps | DisplayPort link RX does not require local crystal for link clock generation. |
| UI_Low_Rate | Unit Interval for Reduced Bit Rate (1.62Gbps/lane) | 613 | 617 | 621 | ps | |
| $V_{RX-DIFFp-p}$ | Differential Peak-to-peak Input Voltage at package pins | 150 | | | mV | Refer to 0 for definition of differential voltage. |
| Rx Horizontal Eye Specification for High Bit Rate | | | | | | |
| $T_{RX-EYE\_CONN}$ | Minimum Receiver Eye Width at Rx-side connector pins | 0.51 | | | UI | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $T_{RX-EYE\_CHIP}$ | Minimum Receiver Eye Width at Rx package pins | 0.47 | | | UI | |
| $T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$ | Maximum time between the jitter median and maximum deviation from the median at Rx package pins | | | 0.265 | UI | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ |
| Rx Horizontal Eye Specification for Reduced Bit Rate | | | | | | |
| $T_{RX-EYE\_CONN}$ | Minimum Receiver Eye Width at Rx-side connector pins | 0.46 | | | UI | |
| $T_{RX-EYE\_CHIP}$ | Minimum Receiver Eye Width at Rx package pins | 0.42 | | | UI | (1- $T_{RX-EYE\_CONN}$) specifies the allowable TJ. |
| $T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$ | Maximum time between the jitter median and maximum deviation from the median at Rx package pins | | | 0.29 | UI | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ |
| $V_{RX-DC-CM}$ | RX DC Common Mode Voltage | 0 | | VDD | V | Common mode voltage is equal to Vbias_Rx voltage shown in Figure 3.8. VDD is the receiver input power supply voltage and 3.6V maximum. |
| $I_{RX-SHORT}$ | RX Short Circuit Current Limit | | | 90 | mA | Total drive current of the transmitter when it is shorted to its ground. |
| $R_{RX-SE}$ | Single-ended RX termination resistance | 45 | 50 | 55 | Ω | |
| $R_{RX-HGIH-IMP-DC}$ | Powered Down DC Input resistance | 200 k | | | Ω | |
| $L_{RX-SKEW-INTER\_CHIP}$ | Lane-to-Lane Skew at RX package pins | | | 5200 | ps | Maximum skew limit between different RX lanes of a DisplayPort link. |
| Intra-pair Skew Specification for High Bit Rate | | | | | | |
| $L_{RX-SKEW-INTRA\_CHIP\_High-Bit-Rate}$ | Lane Intra-pair Skew at RX package pins | | | 100 | ps | Maximum skew limit between D+ and D- of the same lane. |
| Intra-pair Skew Specification for Reduced Bit Rate | | | | | | |
| $L_{RX-SKEW-INTRA\_CHIP\_Reduced-Bit-Rate}$ | Lane Intra-pair Skew at RX package pins | | | 300 | ps | Maximum skew limit between D+ and D- of the same lane. |
| $F_{RX-TRACKING-BW}$ | Jitter Tracking Bandwidth | 20 | | | MHz | Minimum CDR tracking bandwidth at the receiver. |

#### *3.4.2.2 AC Coupling*

Each lane of a DisplayPort link must be AC coupled. The minimum and maximum values for the capacitance are specified in Table 3.7 and Table 3.8. The requirement for the inclusion of AC coupling capacitors on the interconnect media is specified at the DisplayPort transmitter.

#### *3.4.2.3 Termination*

The DisplayPort Main Link transmitter is required to meet the impedance and return loss specifications as specified in Table 3.7, whenever the link is active.

#### *3.4.2.4 DC Common Mode Voltage*

For the DisplayPort Main Link, the transmitter DC common mode voltage is held at the same value during all states unless otherwise specified. The range of allowable transmitter DC common mode values is specified in Table 3.7 ($V_{TX\text{-}DC\text{-}CM}$).

The DisplayPort transmitter shall pre-charge the bus to a common mode voltage for 10 μs or longer before starting Link Training sequence. In the current revision of the Physical Layer specification, an abbreviated version of Link Training following a momentary Electrical Idle period (for example, turning off the link during the vertical blanking interval of a video stream) is not defined.

#### *3.4.2.5 Drive Current and Pre-emphasis*

The DisplayPort transmitter specification allows four (4) drive current levels and four (4) pre-emphasis levels. (Definition of pre-emphasis is shown in Figure 3.10.)Those levels are 8/12/16/24mA and 0/3.5/6.0/9.5dB, respectively. Certain combinations of these result in differential peak-to-peak voltages which are outside the allowable range of $0.4V_{TX\text{-}DIFFp\text{-}p}$ to $1.2V_{TX\text{-}DIFFp\text{-}p}$, and thus, are not allowed. Table 3.9 lists the allowable combinations of drive current and pre-emphasis settings. Pre-emphasis as used in this document is defined as 20 multiplied by the $\log_{10}$ of ratio of the peak-to-peak amplitude for the first $T_{BIT}$ immediately following a transition divided by the peak-to-peak amplitude for the subsequent bits until the next transition ( $20 \cdot \log(Vmax/Vmin)$).

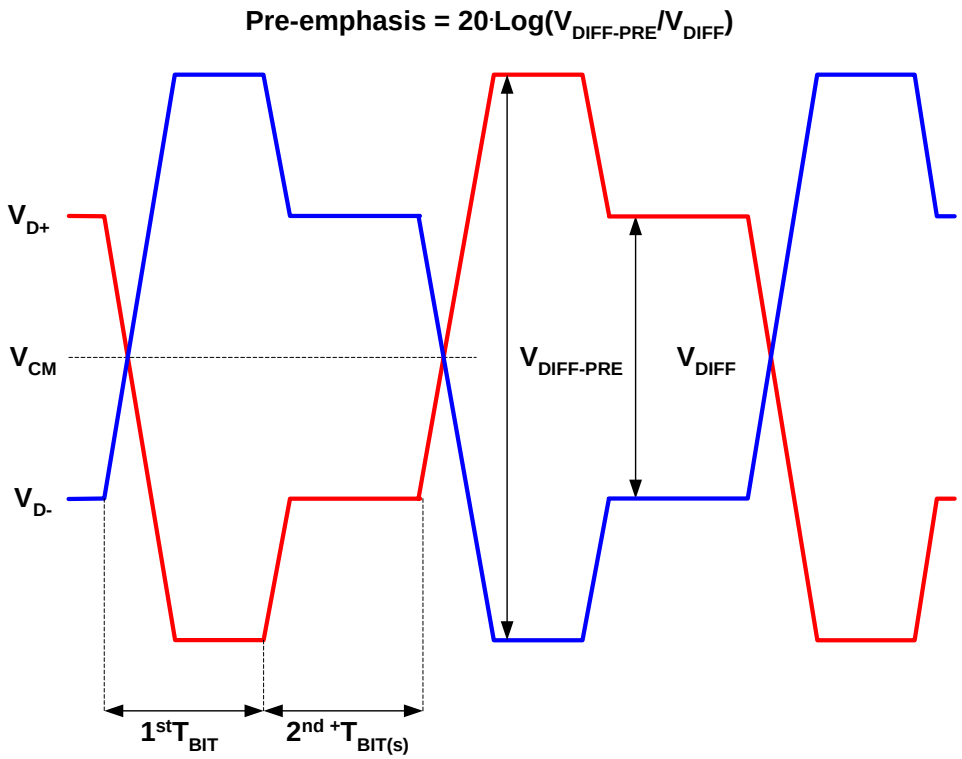



**Figure 3.10 Definition of Pre-emphasis**

**Table 3.9 Allowed Vdiff_pp - Pre-emphasis Combination**

| | Pre-emphasis Level (dB) | | | |
|---|---|---|---|---|
| | 0 dB (1x) | 3.5 dB (1.5x) | 6 dB (2x) | 9.5 dB (3x) |
| | Required | | | Optional |
| Vdiff_pp | Vdiff_pre_pp | Vdiff_pre_pp | Vdiff_pre_pp | Vdiff_pre_pp |
| 0.4 | 0.4 | 0.6 | 0.8 | 1.2 |
| 0.6 | 0.6 | 0.9 | 1.2 | N/A |
| 0.8 | 0.8 | 1.2 | N/A | N/A |
| 1.2 | 1.2 | N/A | N/A | N/A |

### *3.4.2.6 Short Circuit Requirements*

The driver and receiver circuits of Main Link block must survive the worst-case short-circuit current of 90mA (3.6V over 40Ω).

### *3.4.2.7 Bandwidth of Transmitter/Receiver PLL's*

No link clock/reference clock shall be forwarded over the DisplayPort link. Furthermore, no accurate local clock reference shall be assumed in the Sink (receiving) Device. Training Sequence shall be used to establish the proper clock recovery by the DisplayPort receiver.

The DisplayPort specification requires that the Source Device link-clock generation PLL have a closed-loop bandwidth of no more than 4MHz and that the Sink Device clock-recovery PLL have a closed-loop bandwidth of no less than 20MHz (for the D10.2 pattern).

The 4MHz Source Device bandwidth was selected as a reasonable target based on existing designs of a similar nature. The factor-of-five margin was selected to accommodate the lowest dynamic clock recovery bandwidth during the longest ANSI 8B/10B run-lengths.

#### *3.4.2.8 Down-spreading of Link Clock*

Spread spectrum is an optional feature of DisplayPort link. All device timing parameters (including jitter, skew, min-max bit period, output rise/fall time) must meet the existing non-spread spectrum specifications. The preferred method of spreading the link is to apply the spread modulation to the source-clock and subsequently use a clock multiplier to multiply the spread source clock up to the link serializer clock frequency. Spreading that does not allow for modulation above the nominal frequency is often called "down-spreading". Only down-spreading is supported in the DisplayPort specification. The down-spread amplitude shall be either disabled (0.0%) or 0.5% as declared in the DPCD (DisplayPort Configuration Data). The modulation frequency shall be 30- - 33-kHz.

#### *3.4.2.9 Sampling Jitter Specifications*

##### 3.4.2.9.1 Jitter output/tolerance mask

The DisplayPort spectral jitter shall comply with the requirements as indicated in the Jitter Output/Tolerance Graph, shown in Figure 3.11 – Jitter output/tolerance mask. $A_x$ are the maximum peak to peak transmitter output and the minimum peak to peak receiver tolerance requirements as measured from an edge to any following edge up to $n_x$ times UI later (where x is 0,1, or 2 in corresponding to the high, mid, and low frequency break-points of the jitter tolerance mask, and differential noise budget table).

Transmitter output edge timing variation from $t_0$ to $t_y$ shall not exceed the value computed by the following:

- y is an integer from 1 to $n_x$,
- $t_y$ is the time of the edge measurement for a transition y*UI bit periods after the edge at time $t_0$

This measurement can be made with an oscilloscope having a histogram function or with a Timing Interval Analyzer (TIA). A receiver must be able to tolerate the peak to peak jitter specified.

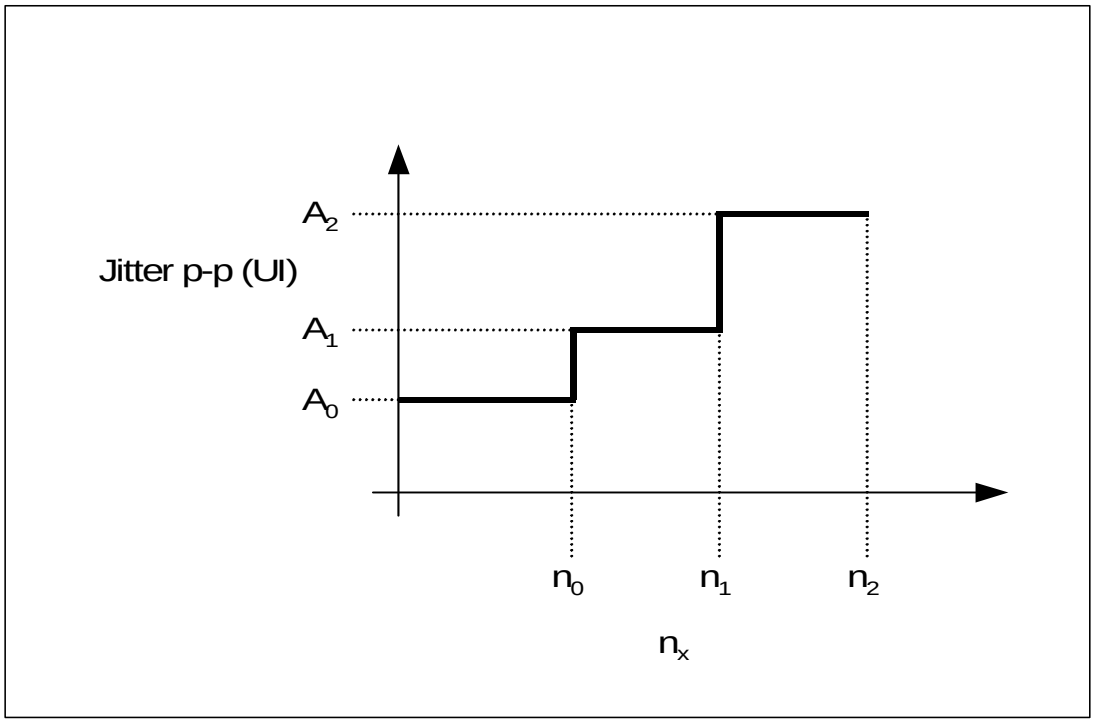



**Figure 3.11 Jitter output/tolerance mask**

#### 3.4.2.9.2 Sampling differential noise budget

Sampling jitter specifications relate to the relationship between the sampling clock and the data. Any phase error that results in the sample being improperly read (i.e. prior bit or following bit sampled) will result in a bit error.

These error components have been broken out into Deterministic Jitter (DJ) and Total Jitter (TJ) where appropriate. DJ is the peak to peak phase variation in the $0V_{differential}$ crossing point of the data stream that is fixed given any specific set of conditions. TJ is defined as DJ + Random Jitter (RJ). RJ is defined as 12.3 times the rms (1 sigma) value of the jitter that is Gaussian (normal). The DisplayPort interface jitter characteristics should comply with the jitter budget allocations tabulated in Table 3.10.

**Table 3.10 Sampling Differential Noise Budget**

| | Transmitter output[1] | | Transmitter Connector | | Receiver Connector | | Receiver input[2] | | Note reference |
|---|---|---|---|---|---|---|---|---|---|
| | DJ | TJ | DJ | TJ | DJ | TJ | DJ | TJ | |
| High-Bit Rate (2.7Gbps per lane) | | | | | | | | | |
| $A_{0,p-p}$ | 0.080 | 0.260 | 0.132 | 0.312 | 0.311 | 0.491 | 0.350 | 0.530 | 3, 4 |
| $n_0$ | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 3, 4 |
| $A_{1,p-p}$ | 0.130 | 0.380 | 0.182 | 0.432 | 0.441 | 0.691 | 0.480 | 0.730 | 3, 5 |
| $n_1$ | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 3, 5 |
| $A_{2,p-p}$ | 40 | | 40 | | 40 | | 40 | | 6, 7 |
| $n_2$ | 25000 | | 25000 | | 25000 | | 25000 | | 6, 7 |
| Reduced-Bit Rate (1.62Gbps per lane) | | | | | | | | | |
| $A_{0,p-p}$ | 0.050 | 0.160 | 0.093 | 0.203 | 0.429 | 0.539 | 0.470 | 0.580 | 3, 4 |
| $n_0$ | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3, 4 |
| $A_{1,p-p}$ | 0.080 | 0.230 | 0.123 | 0.273 | 0.639 | 0.789 | 0.680 | 0.830 | 3, 5 |
| $n_1$ | 150 | 150 | 150 | 150 | 150 | 150 | 150 | 150 | 3, 5 |
| $A_{2,p-p}$ | 24 | | 24 | | 24 | | 24 | | 6, 7 |
| $n_2$ | 15000 | | 15000 | | 15000 | | 15000 | | 6, 7 |

**Notes**:

1. The transmitter output is the maximum jitter that the transmitter may exhibit to guarantee operation.
2. The receiver input is the maximum jitter that a receiver must tolerate to guarantee operation.
3. Does not include frequency error due to frequency skew (XTAL or SSC related).
4. Primarily determined by over-sampled architecture requirements.
5. Primarily determined by tracking architecture requirements.
6. For low frequency (track-able) jitter, total jitter is specified (DJ is not broken out).
7. Primarily determined by Spread Spectrum Clocking (+/-0.25% AC portion). Does not include the -0.25% fixed skew (additional 26 UI).

#### 3.4.2.9.3 Relationship of frequency to the jitter specification (INFORMATIVE)

Successful compliance with the EYE diagram metric presented earlier is not sufficient to guarantee compliance with the jitter budget. Therefore it is essential to examine the jitter specification as a function of frequency. This section is provided as clarifying information. Figure 3.11 shows a plot of the maximum amplitude (in UI) sine wave at a given frequency that satisfies all the jitter specifications and the calculations leading to this graph.

As for the A2 and n2 (the 25000UI jitter) data point described in Figure 3.11 (figuratively) and Table 3.10,, the measurement shall be triggered using the receiver's recovered clock test output described in Section 3.4.1.5 on page 132. This is not intended for generating an eye mask.

**Jitter specification at the receiver input**

$A_0 = 0.5$ $A_1 = 0.73$ $A_2 = 40$

$n_0 = 5$ $n_1 = 250$ $n_2 = 25000$

**Frequency of sine wave with peak values separated by n data rate cycles**

$$datarate := 2.7 \cdot 10^9$$

$$f(n) := \frac{datarate}{2 \cdot n}$$

**Maximum amplitude of a sine wave with frequency f(n) and a slew rate constrained by jitter spec n x,ax**

$$a(n, n_x, a_x) := \frac{a_x}{\sin\left(\frac{\pi \cdot n_x}{2 \cdot n}\right)}$$

**Maximum compliant peak-to-peak amplitude**

$$p(n) := \begin{cases} A0 & \text{if } (n \le N0) \\ (\min((a(n, N0, A0)\ \ A1))) & \text{if } (n > N0) \cdot (n \le N1) \\ (\min((a(n, N1, A1)\ \ A2))) & \text{if } (n > N1) \\ 0 & \text{otherwise} \end{cases}$$

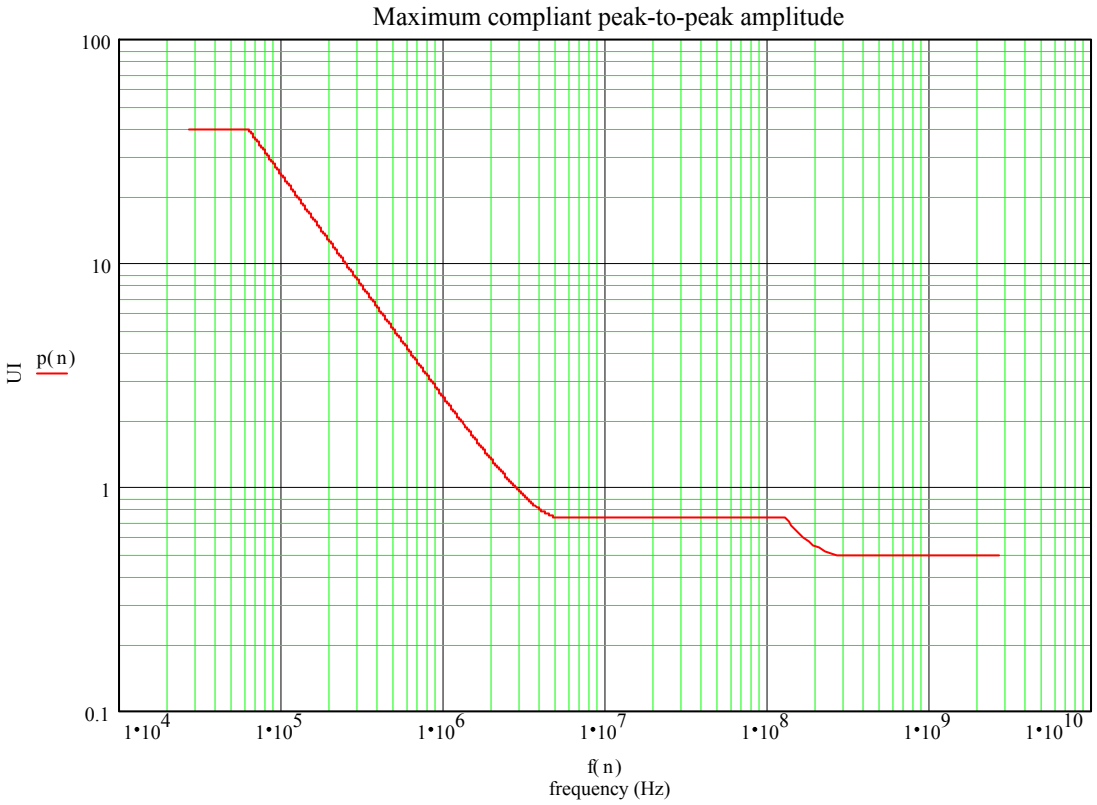



**Figure 3.12 Jitter as a function of frequency**

A compliant Source (transmitter) shall have the entire jitter spectrum at or below this curve, whereas a compliant Sink (receiver) must tolerate at least the amount of jitter spectrum shown in Figure 3.12.

### 3.4.2.9.4 Sampling BER and jitter formulas

The values for RJ and DJ above are calculated using the following relationship between BER and jitter. This is provided for reference and not intended for use as a compliance requirement. The over-sampling formula assumes a worse-case oversampling ratio (osr) of three and sets the $A_0,n_0$ jitter requirements. The tracking architecture sets the $A_1,n_1$ requirement. $A_2,n_2$ is set to guarantee SSC compliance. Also shown below are $DJ_{RX}$ and $RJ_{RX}$ numbers for the two architectures. These are example budgets for the local receiver that satisfies the $10^{-9}$ BER goal.

**Gaussian Distribution Error Function**

$$G(x) := \frac{1}{\sqrt{2\cdot\pi}}\cdot\int_0^x e^{\frac{-\xi^2}{2}}\,d\xi + 0.5 \qquad x>0$$

**The above equation is simplified to the closed form:**

$$G(x) := \frac{1}{2}\cdot\mathrm{erf}\left(\frac{1}{2}\cdot\sqrt{2}\cdot x\right) + .5$$

**Bit Error Rate Due to Sampling (tracking architecture)**

$DJ_{RX} := 0.15 \qquad RJ_{RX} := 0.18$

$DJ := 0.48 + DJ_{RX} \qquad RJ := 0.25 + RJ_{RX}$

$$BER_{tr} := 2 - G\left[7\cdot\frac{(1-DJ)}{RJ}\right] - G\left[7\cdot\frac{(1+DJ)}{RJ}\right]$$

$BER_{tr} = 8.547\cdot 10^{-10}$

**Bit Error Rate Due to Sampling (oversampling architecture)**

$osr := 3$

$DJ_{RX} := 0.08 \qquad RJ_{RX} := 0.09$

$DJ := 0.35 + DJ_{RX} \qquad RJ := 0.18 + RJ_{RX}$

$$BER_{tr} := 2 - G\left[7\cdot\frac{(2-DJ\cdot osr)}{RJ\cdot osr}\right] - G\left[7\cdot\frac{(2+DJ\cdot osr)}{RJ\cdot osr}\right]$$

$BER_{tr} = 4.237\cdot 10^{-10}$

### *3.4.2.10 Differential voltage/timing (EYE) diagram*

The EYE diagram is used to measure compliance of the signal into the test load for the specified number of UI's. It must be noted that while the EYE is a compliance measurement, it does not guarantee that the jitter specification has been met. Jitter requirements listed elsewhere in this specification must be met in addition to the eye diagram to comply with this specification. Down-spreading of the link clock should be disabled for the capture of data to be used with the EYE masks.

The masks in Figure 3.13 show two polygons. The dashed-outer polygons represent the 5UI mask and the solid-inner polygons represent the 250UI eye mask. Table 3.11 and Table 3.12 contain the values to be used for the vertices of the mask.

The diagram may be created using multiple samples, but each sample must be of the specified capture length and normalized to the average UI of the sample interval.

It should be noted that some DisplayPort receivers may be able to support a receiver eye opening that is smaller than the Receiver EYE Masks shown in Figure 3.14 on p. 148 by, for example, implementing an equalizer. Vendors of such receivers may publish the Receiver Eye Masks at the receiver package pins that are smaller than those in Figure 3.14 . Table 3.13 and Table 3.14 contain the values to be used for the vertices of the mask.

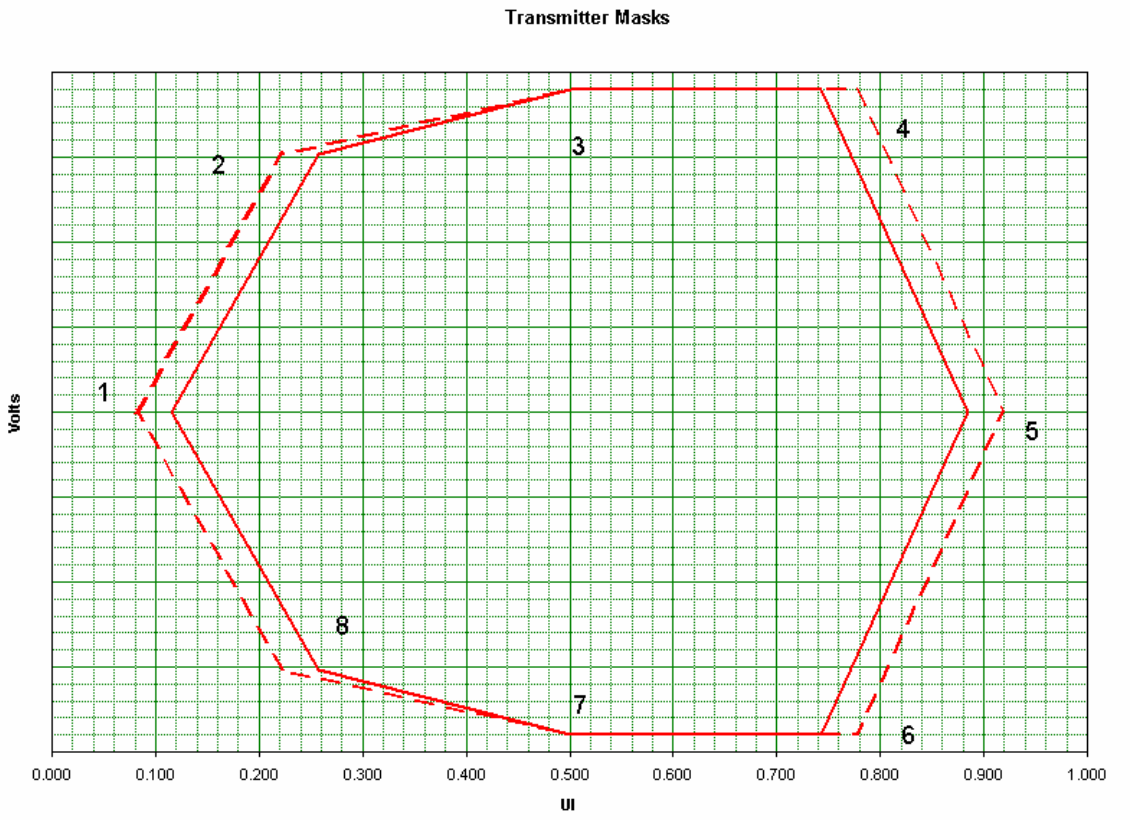



**Figure 3.13 Transmit EYE Mask**

**Table 3.11 Mask Vertices Table for High Bit Rate**

| Point | Time: 5 UI | Time: 250 UI | Voltage Level 1 (Volts) | Voltage Level 2 (Volts) | Voltage Level 3 (Volts) | Voltage Level 4 (Volts) |
|---|---|---|---|---|---|---|
| 1 | 0.130 | 0.190 | 0.000 | 0.000 | 0.000 | 0.000 |
| 2 | 0.272 | 0.332 | 0.152 | 0.228 | 0.304 | 0.456 |
| 3 | 0.500 | 0.500 | 0.190 | 0.285 | 0.380 | 0.570 |
| 4 | 0.728 | 0.668 | 0.190 | 0.285 | 0.380 | 0.570 |
| 5 | 0.870 | 0.810 | 0.000 | 0.000 | 0.000 | 0.000 |
| 6 | 0.728 | 0.668 | -0.190 | -0.285 | -0.380 | -0.570 |
| 7 | 0.500 | 0.500 | -0.190 | -0.285 | -0.380 | -0.570 |
| 8 | 0.272 | 0.332 | -0.152 | -0.228 | -0.304 | -0.456 |

**Table 3.12 Mask Vertices Table for Reduced Bit Rate**

| Point | Time: 5 UI | Time: 250 UI | Voltage Level 1 (Volts) | Voltage Level 2 (Volts) | Voltage Level 3 (Volts) | Voltage Level 4 (Volts) |
|---|---|---|---|---|---|---|
| 1 | 0.080 | 0.115 | 0.000 | 0.000 | 0.000 | 0.000 |
| 2 | 0.222 | 0.257 | 0.152 | 0.228 | 0.304 | 0.456 |
| 3 | 0.500 | 0.500 | 0.190 | 0.285 | 0.380 | 0.570 |
| 4 | 0.778 | 0.743 | 0.190 | 0.285 | 0.380 | 0.570 |
| 5 | 0.920 | 0.885 | 0.000 | 0.000 | 0.000 | 0.000 |
| 6 | 0.778 | 0.743 | -0.190 | -0.285 | -0.380 | -0.570 |
| 7 | 0.500 | 0.500 | -0.190 | -0.285 | -0.380 | -0.570 |
| 8 | 0.222 | 0.257 | -0.152 | -0.228 | -0.304 | -0.456 |

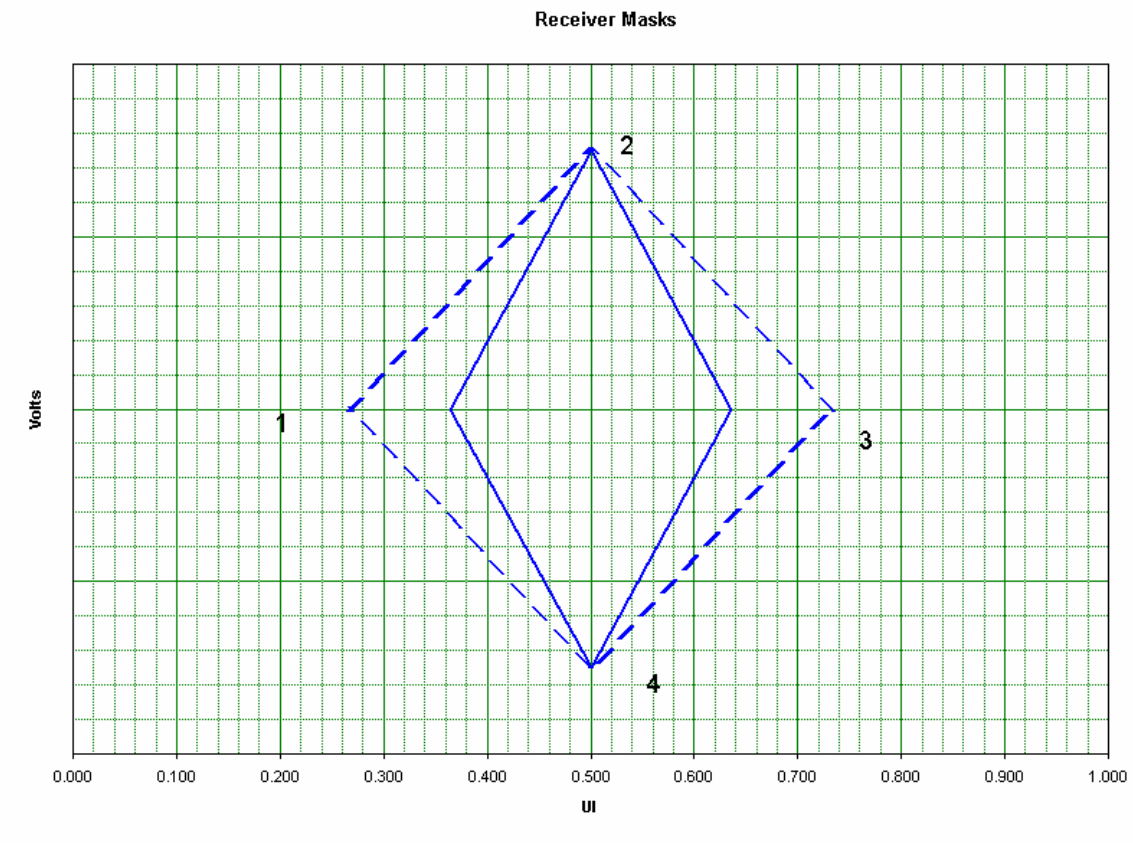



**Figure 3.14 Receive EYE Mask**

**Table 3.13 Receiver Mask Vertices Table for High Bit Rate**

| Point | Time: 5 UI | Time: 250 UI | Voltage |
|---|---|---|---|
| 1 | 0.265 | 0.365 | 0.000 |
| 2 | 0.500 | 0.500 | 0.075 |
| 3 | 0.735 | 0.635 | 0.000 |
| 4 | 0.500 | 0.500 | -0.075 |

**Table 3.14 Receiver Mask Vertices Table for Reduced Bit Rate**

| Point | Time: 5 UI | Time: 250 UI | Voltage |
|---|---|---|---|
| 1 | 0.290 | 0.415 | 0.000 |
| 2 | 0.500 | 0.500 | 0.075 |
| 3 | 0.710 | 0.585 | 0.000 |
| 4 | 0.500 | 0.500 | -0.075 |

### 3.4.3 ESD and EOS Protection

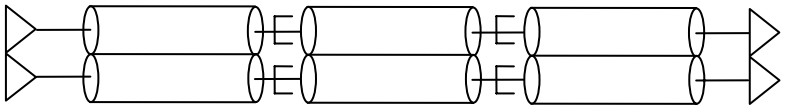
The DisplayPort based system shall protect all potentially exposed interface signals and power pins to meet or exceed the EOS (electrical over stress) specification of IEC 61000-4-2, Level 4 (8kV Contact) without damage. For repeatability of the contact test, the exposed I/O or power line must withstand a direct strike to each connector pin without contacting the ESD test gun to the connector shield.

All signal and power pins of associated DisplayPort components (transmitter IC, receiver IC, and associated I/O circuitry) shall also withstand at least JEDEC JESD22-A114-B Class 2 (2kV Human Body Model, 200V Machine Model) strikes.

DisplayPort Devices implementing this specification may swing I/O lines as high as +/-0.3V single-ended with respect the common mode bias reference level. The designer shall carefully select clamping devices and clamping rail voltages such that ESD devices will not cause clipping of normal signals.

### 3.4.4 Channel Budget at Source/Sink Connectors (for Box-to-Box)

This section describes the electrical requirements of the printed circuit routing between the Main Link chip pins and the corresponding connectors for both the Source and Sink Devices. They are referred to as "Source Interconnect" and "Sink Interconnect" in Figure 3.15, respectively. Throughout this section, the compliance test load consists of a pair of 50Ω resistive loads as shown in Figure 3.16.



| Transmitter Chip Pins | Source Interconnect | MP2 | Cable | MP3 | Sink Interconnect | Receiver Chip Pins |
|---|---|---|---|---|---|---|

**Figure 3.15 Compliance Measurement Points of the Channel**

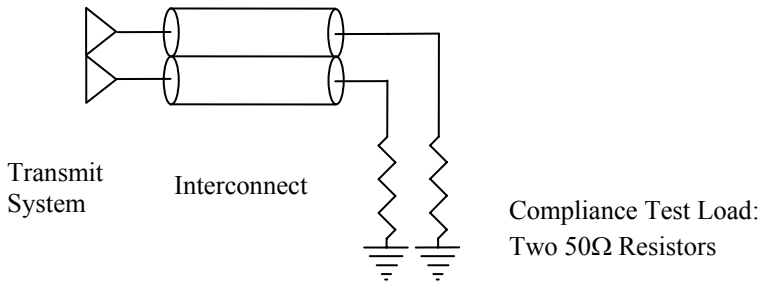



**Figure 3.16 Compliance Test Load**

#### *3.4.4.1 Interconnect between Main Link Tx Chip Pins and Source Connector*

The Source Interconnect between the Source connector (MP2 in Figure 3.15 and the Main Link transmitter chip pins shall be a network consisting of 100Ω differential nominal impedance with +/-10% tolerance. Protection devices shall add no more than 1.5pF parasitic load to each trace. Series protection resistors are not recommended. Losses are demonstrated by an EYE measurement at the Source connector.

**Note**: The approximate maximum length is 12 inches (304.5mm) using high volume manufacturing PCB materials. It is recommended that no more than three vias per trace be used.

### *3.4.4.2 Main Link EYE Masks at Source Connector*

The EYE diagram shall be used to measure compliance of the signal into the test load for the specified number of UI's. The Source connector EYE shall be tested at MP2 in Figure 3.15 with the compliance test load as shown in Figure 3.16. The masks shall be measured with the DisplayPort transmitter set at the highest required specified drive setting (0.8Vdiffp-p) and at with no pre-emphasis (0dB). All Main Link lanes shall be on and driving the PRBS7 test pattern with a two symbol (20UI) skew between each lane and adjacent lane(s).

Note that while the EYE is a compliance measurement, it does not guarantee that the jitter specification has been met. Jitter requirements listed in Section 3.4.2.9 on p.141 shall be met in addition to the eye diagram to comply with this specification. Down-spreading of the link clock shall be disabled for the capture of data to be used with the EYE masks.

Figure 3.17 shows two polygons. The dashed-outer polygons represent the 5UI mask and the solid-inner polygons represent the 250UI eye mask. Table 3.15 and Table 3.16 contain the values to be used for the vertices of the mask for determining compliance/non-compliance.

The diagram may be created using multiple samples, but each sample, 5bit and 250bit, must be of the specified capture length and normalized to the average UI of the sample interval.

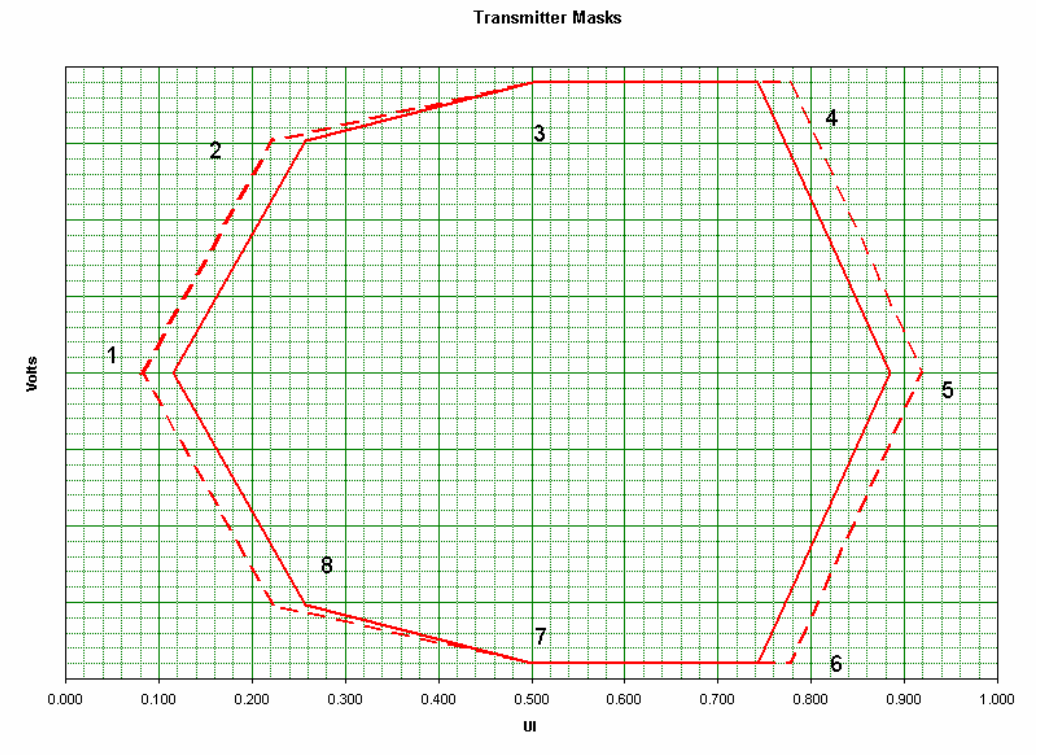



**Figure 3.17 Main Link EYE Masks at Source Connector**

**Table 3.15 Main Link EYE Mask Vertices Table for High Bit Rate at Source Connector**

| Point | Time: 5 UI | Time: 250 UI | Voltage Level (Volts) |
|---|---|---|---|
| 1 | 0.143 | 0.200 | 0.000 |
| 2 | 0.347 | 0.395 | 0.125 |
| 3 | 0.545 | 0.545 | 0.186 |
| 4 | 0.622 | 0.564 | 0.186 |
| 5 | 0.858 | 0.800 | 0.000 |
| 6 | 0.622 | 0.564 | -0.186 |
| 7 | 0.545 | 0.545 | -0.186 |
| 8 | 0.347 | 0.395 | -0.125 |

**Note**: Measured at MP2 in Figure 3.15 with 0.8Vdiff_p-p drive, no pre-emphasis.

**Table 3.16 Main Link EYE Mask Vertices Table for Reduced Bit Rate at Source Connector**

| Point | Time: 5 UI | Time: 250 UI | Voltage Level (Volts) |
|---|---|---|---|
| 1 | 0.093 | 0.125 | 0.000 |
| 2 | 0.224 | 0.256 | 0.131 |
| 3 | 0.445 | 0.445 | 0.228 |
| 4 | 0.764 | 0.731 | 0.228 |
| 5 | 0.908 | 0.875 | 0.000 |
| 6 | 0.764 | 0.731 | -0.228 |
| 7 | 0.445 | 0.445 | -0.228 |
| 8 | 0.224 | 0.256 | -0.131 |

**Note**: Measured at MP2 in Figure 3.15 with 0.8Vdiff_p-p drive, no pre-emphasis.

### *3.4.4.3 Sink Connector to Main Link Receiver Chip Pins*

The Sink Interconnect between the Sink connector (MP3 in Figure 3.15) and the Main Link receiving chip pins shall be a network consisting of 100Ω differential nominal impedance with a +/-10% tolerance and a delay of no more that 380ps. Protection devices shall add no more than 1.5pF parasitic load to each trace. Series protection resistors are not recommended.

**Note**: The approximate maximum length is 2 inches (50.8mm) using high volume manufacturing PCB materials. It is recommended that no more than two vias per trace be used.

The receive EYE shall be tested by feeding a test pattern from MP3 in Figure 3.15 using a pattern generator with voltage swing and rise time configured to generate the minimum specified EYE at the Sink. This pattern shall be PRBS7 running at 1.35GHz (2.7Gbps) with 1V_diff_pp (or 500mV single ended) and the rise/fall time of 100 ps from 20-80%. The values specified in Table 3.17 shall be used to determine compliance/non-compliance. Measurements shall be taken at the point where the Main Link receiver chip pins attach to the board with compliance test load as shown in Figure 3.16, with the receiver chip removed.

Note that while the EYE is a compliance measurement, it does not guarantee that the jitter specification has been met. Jitter requirements listed in Section 3.4.2.9 on p.141 shall be met in addition to the eye diagram to comply with this specification.

Figure 3.18 shows two polygons. The dashed-outer polygons represent the 5UI mask and the solid-inner polygons represent the 250UI eye mask. Table 3.17 contains the values to be used for the vertices of the mask for determining compliance/non-compliance.

The diagram may be created using multiple samples, but each sample, 5bit and 250bit, must be of the specified capture length and normalized to the average UI of the sample interval.

Refer to the DisplayPort compliance document for test equipment requirements and recommendations, test load adaptor fixture requirements and design details, and other measurement procedure details.

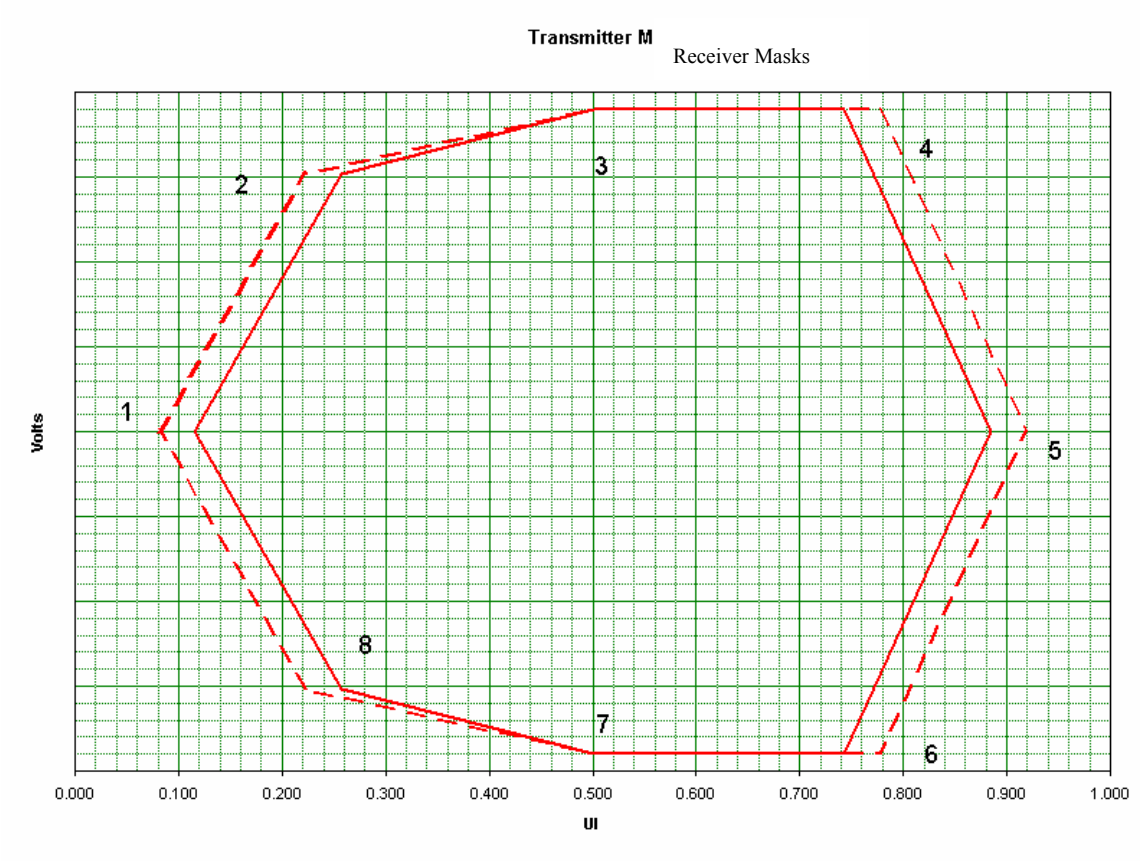



**Figure 3.18 EYE Masks at Main Link Receiver Chip Pins for Testing Sink Interconnect**

**Table 3.17 Vertices of EYE Masks at Main Link Receiver Chip Pins for Testing Sink Interconnect**

| Point | Time: 5 UI | Time: 250 UI | Voltage Level (Volts) |
|---|---|---|---|
| 1 | 0.064 | 0.122 | 0.000 |
| 2 | 0.221 | 0.273 | 0.243 |
| 3 | 0.520 | 0.520 | 0.380 |
| 4 | 0.805 | 0.747 | 0.380 |
| 5 | 0.937 | 0.879 | 0.000 |
| 6 | 0.805 | 0.747 | -0.380 |
| 7 | 0.520 | 0.520 | -0.380 |
| 8 | 0.221 | 0.273 | -0.243 |

**Note**: This is not for a complete test. It is for interconnect within Sink Device only.

### 3.4.5 Internal Connection (within a single box)

The receiver eye mask for the internal (that is, within a single box) connection shall be measured at the Main Link receiver chip pins. The EYE mask described in Figure 3.14 on p. 148 shall be used to determine compliance/non-compliance. The test shall be conducted on the complete channel with the Main Link transmitter chip driving the Symbol Error Rate Measurement Pattern described in Section 2.5.3.5.2 on p.109. Measurements shall be taken at the point where the Main Link receiver chip pins attach to the board with a compliance test load as shown in 0 with receiver chip removed.

Note that while the EYE is a compliance measurement, it does not guarantee that the jitter specification has been met. Jitter requirements listed in Section 3.4.2.9 on p.141 shall be met in addition to the eye diagram to comply with this specification. Down-spreading of the link clock shall be disabled for the capture of data to be used with the EYE masks. Pre-emphasis and drive levels may be set to any available value to achieve success.

The diagram may be created using multiple samples, but each sample, 5bit and 250bit, must be of the specified capture length and normalized to the average UI of the sample interval.

.

# 4 Mechanical

This chapter describes the mechanical specifications of DisplayPort link. Cable assembly specification for external connection and connector specification are covered in this chapter[2].

## *4.1 Cable-Connector Assembly Specifications (for box-to-box)*

The cable assembly specification is divided into two categories reflecting the high bit rate (2.7Gbps per lane) and the low bit rate (1.62Gbps per lane), respectively.

The high bit rate specification in general has higher performance electrical requirements and is usually represented by one or more of the following: shorter lengths, larger wire gauges, lower dielectric loss insulation materials. The low bit rate specification in general has lower performance electrical requirements and is usually represented by one or more of the following: longer lengths, smaller wire gauges, higher dielectric loss insulation materials. Among the cable-connector assembly parameters, IL (insertion loss), RL (reflection loss), skew (both intra-pair and inter-pair), and Near End Noise (NEN) differ between high-bit-rate and low-bit-rate specifications.

Both categories represent the box-to-box application space sometimes referred to as external/desktop and consumer electronics (CE). The embedded cable application space which is characterized by its inaccessibility to the end-user and is sometimes referred to as internal/mobile is not explicitly specified herein; instead, the system-integrator is required to meet the EYE mask requirements at the receiver pins by making appropriate trade-offs between circuit trace performance and cabling performance. In general the high bit rate and low bit rate electrical specification presented below still apply to the internal/mobile cable assemblies given the same FR4 routes at both ends of the channel except that the physical dimensions are much smaller.

[2] Masks for insertion loss, reflection loss, near-end noise, and far-end noise, and the impedance profile in this chapter were generated by Tyco Electronics. Channel simulations were run to verify that the worst-case cable-connector assembly as represented by those masks would meet receiver eye masks specified in this document.

### 4.1.1 Cable-Connector Assembly Definition

DisplayPort Cable Assembly is defined as two plug types of connectors terminating both ends of a bulk cable together comprises a cable assembly as depicted in Figure 4.1.

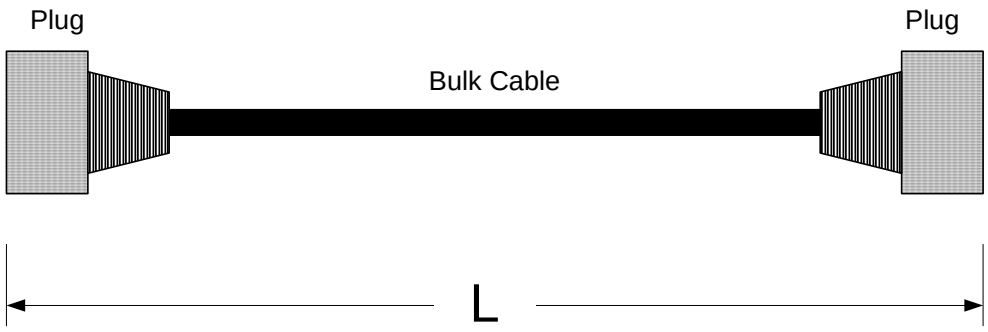



**Figure 4.1 Cable Assembly**

### 4.1.2 Type of bulk cable

The bulk cable shall be chosen to meet or exceed all of the electrical and mechanical requirements described herein. A reference construction is depicted in Figure 4.2 below.

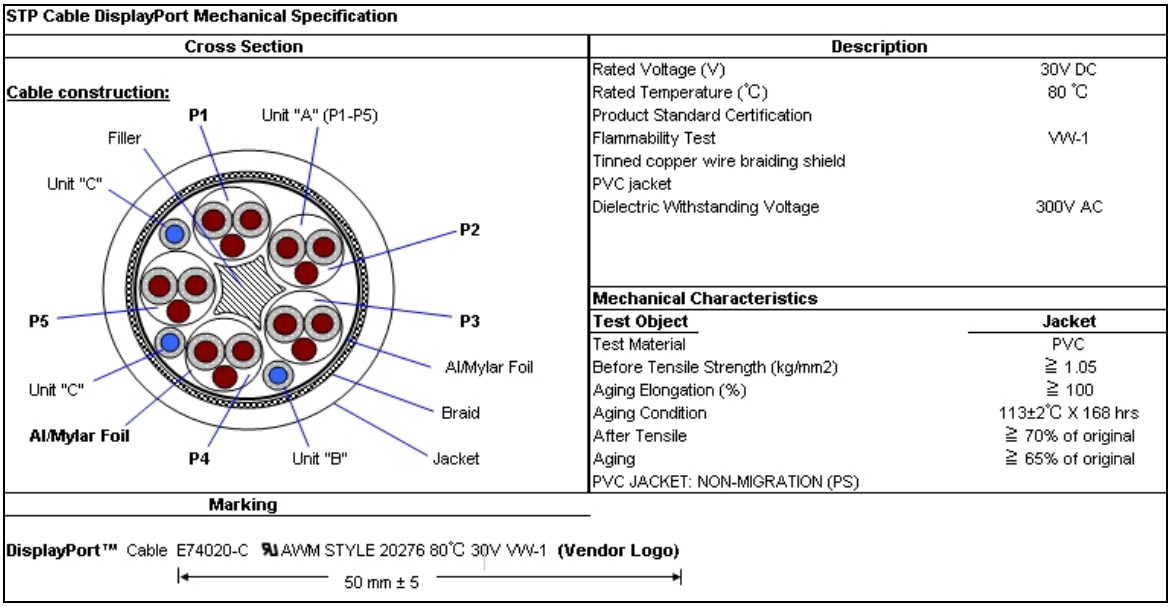



**Figure 4.2 Bulk Cable Specification**

- Overall Shielded (Braid) structure coated with jacket above
- Unit “A”: P1-P5 ‘STP’ #30 AWG insulated stranded conductors, with #30 AWG Drain conductor
- Unit “B”: ‘Unshielded, #30 AWG single insulated stranded conductor.
- Unit “C”: ‘Unshielded, #28 or #30AWG single insulated stranded conductor.

**Note**: Since unit “C” is for power purpose and very short distance from the connector, it is recommended to use the power as #30AWG “STP” structure with no drain wire, rather than two single-ended conductors.

### 4.1.3 Impedance Profile

Impedance specification shall be defined in a time domain. The impedance profile shall be measured using controlled impedance fixture and TDR with differential sampling head. The fixture rise time shall be 50ps (20% - 80%) or faster while readout of measurement shall be filtered to tr = 110 ps (20% - 80%). Impedance values shall conform to those listed in Table 4.1. Figure 4.3 shows an example of measured data.

**Table 4.1 Impedance profile values for Cable Assembly**

| Segment | Differential Impedance Value | Maximum Tolerance | Comment |
|---|---|---|---|
| Fixture | 100 Ω | ± 10% | Fixture shall have traces lengths of no more than 5cm (2”) |
| Connector | 100 Ω | | |
| Wire Management | 100 Ω | | |
| Cable | 100 Ω | ± 5% | |

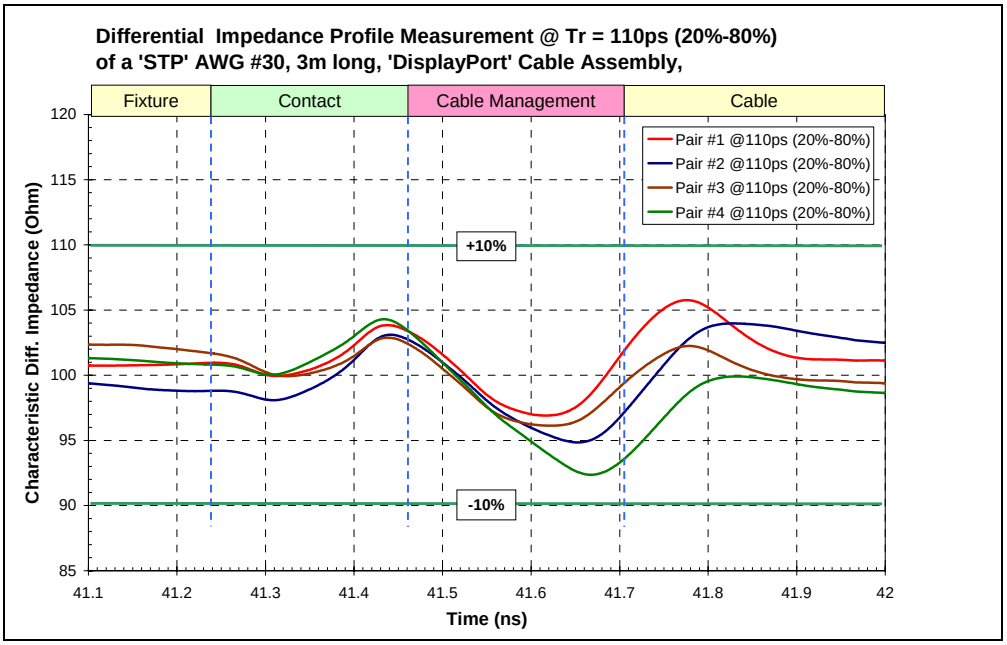



**Figure 4.3 Impedance Profile Measurement Data Example**

### 4.1.4 Insertion Loss & Return Loss

Insertion Loss and Return Loss specified in this chapter are the mixed mode S-Parameters known as SDD21 and SDD11, respectively. Unlike Single Ended case, SDDij refers to differential stimulus & differential response as illustrated in the following matrix of all mixed modes in differential case as shown in Table 4.2.

**Table 4.2 Mixed Mode Differential / Common relations of S-Parameters**

| | | Stimulus | | | |
|---|---|---|---|---|---|
| | | Differential | | Common | |
| Response | Differential | SDD11 | SDD12 | SDC11 | SDC12 |
| | | SDD21 | SDD22 | SDC21 | SDC22 |
| | Common | SCD11 | SCD12 | SCC11 | SCC12 |
| | | SCD21 | SCD22 | SCC21 | SCC22 |

## 4.1.5 High-bit-rate Cable-Connector Assembly Specification

### *4.1.5.1 Insertion Loss & Return Loss*

The following equations represents the reference line that limits the 'Insertion Loss' and 'Return Loss' measured results.

#### 4.1.5.1.1 Insertion Loss Lower Limit for High Bit Rate Cable Assemblies:

$$IL_{\min.}[dB] = \begin{cases} -8.7 \times \sqrt{\frac{f}{f_0}} & ; \quad 0.1 < f \le \frac{f_0}{3} \\ -4.9 \times \left( \frac{3f - f_0}{3} \right) - 5 & ; \quad \frac{f_0}{3} < f \le 7 \end{cases}$$

Where:

$f$ is given in *GHz*

$f_0$ = 1.35 *GHz*

#### 4.1.5.1.2 Return Loss Upper Limit for High Bit Rate Cable Assemblies:

$$RL_{\max.}[dB] = \begin{cases} -15 & ; \quad 0.1 < f \le \frac{f_0}{2} \\ -15 + 12.3\ Log_{10}\left(\frac{2f}{f_0}\right) & ; \quad \frac{f_0}{2} < f \le 7 \end{cases}$$

Where:

$f$ is given in *GHz*

$f_0 = 1.35$ *GHz*

Figure 4.4 and Figure 4.5 depict the charts that represent the above mentioned equations 'Insertion Loss' and 'Return Loss' respectively, and shall be referenced as the lower limit for 'Insertion Loss' and upper limit for 'Return Loss' respectively.

The cable assembly measured results shall comply with these limits.

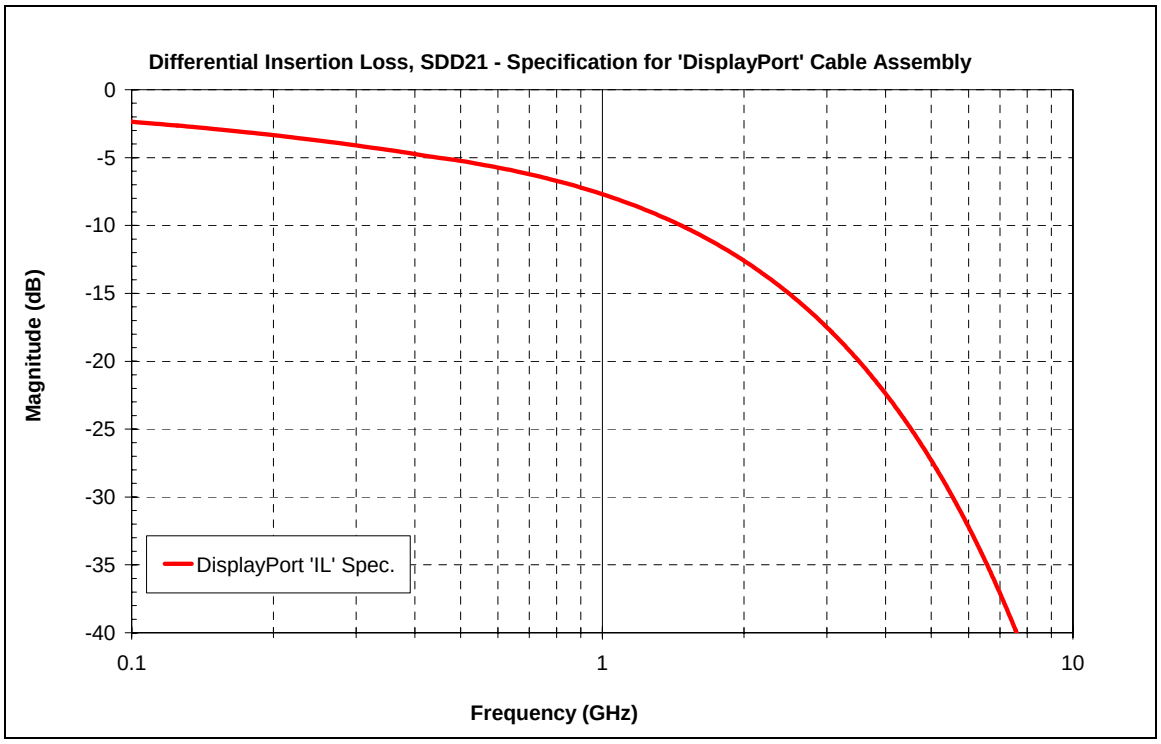



**Figure 4.4 Mixed Mode Differential Insertion Loss for High-bit-rate Cable Assembly**

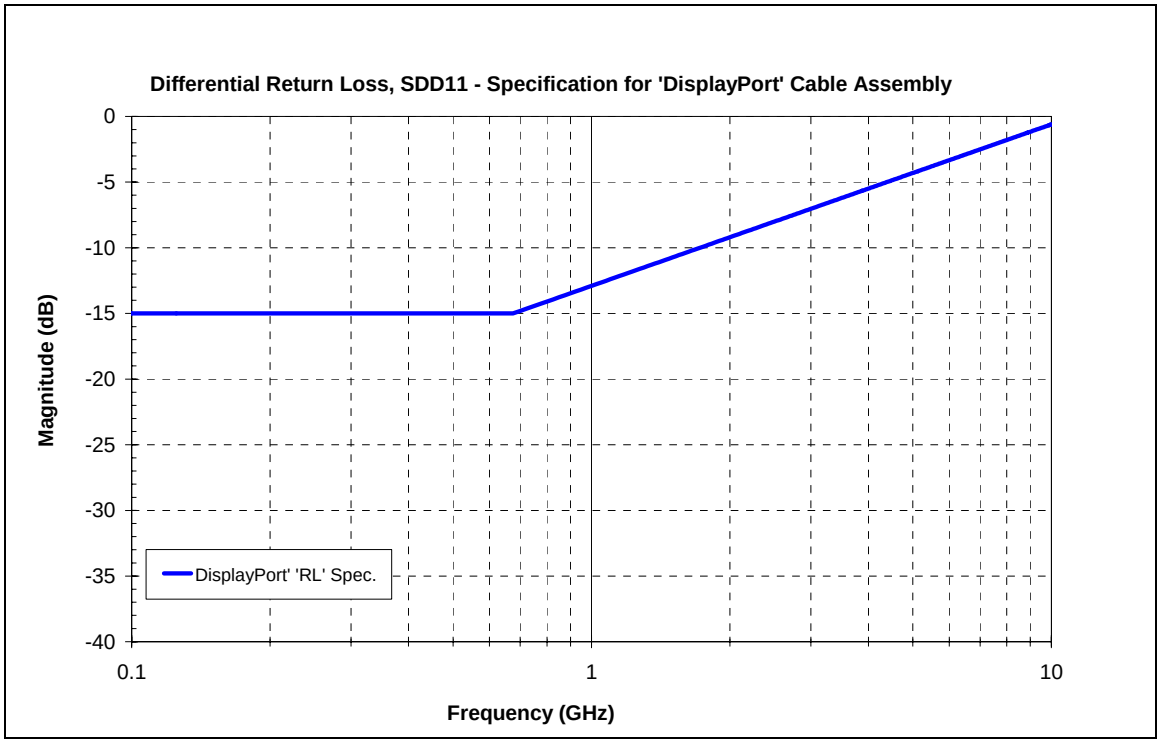



**Figure 4.5 Mixed Mode Differential Return Loss for High-bit-rate Cable Assembly**

### *4.1.5.2 Near End Noise (NEN)*

Near End Noise (NEN) shall be defined in frequency domain and cover the bandwidth of up to 7GHz. The NEN shall be lower than the upper limit in the Isolation equation and depicted in Figure 4.6 below:

**Near End Noise - Upper Limit for 3m Long, High Speed Cable Assembly:**

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 7 \end{cases}$$

Where:

$f$ is given in *GHz*

$f_0$ = 1.35 *GHz*

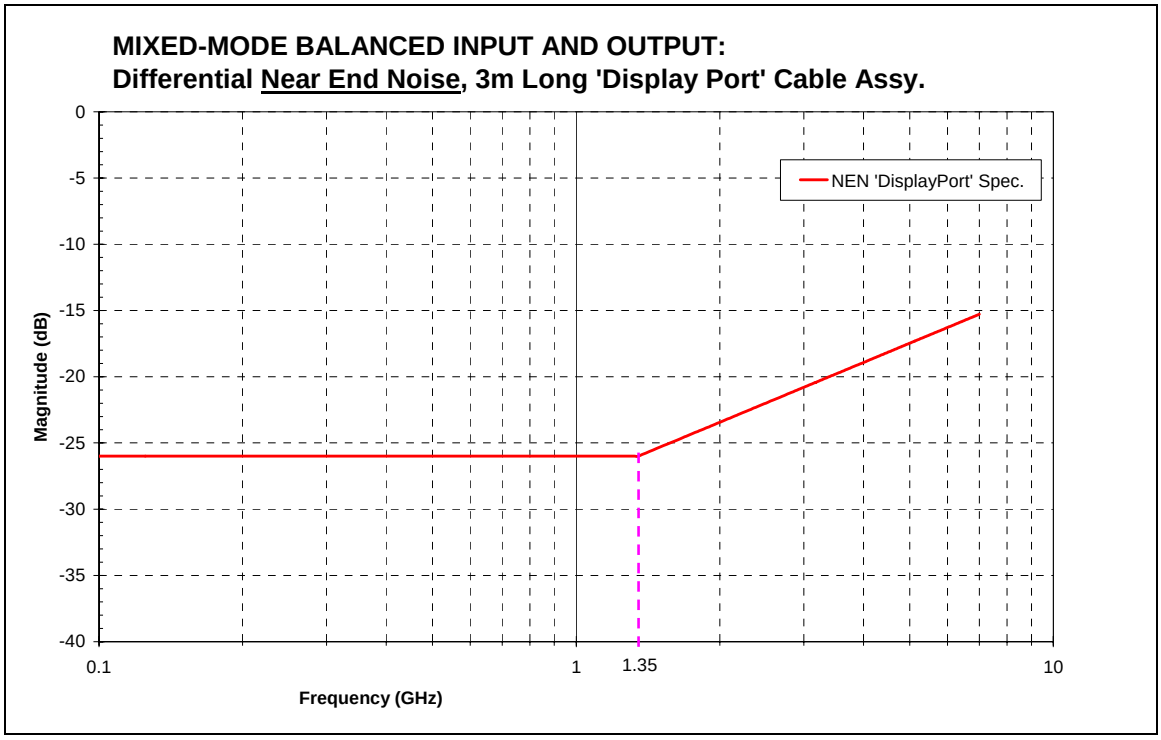



**Figure 4.6 Near End Total Noise (peak) for High-bit-rate Cable Assembly**

### *4.1.5.3 Far End Noise (FEN)*

The Far End Noise shall be lower than the upper limit as depicted in Figure 4.7 below:

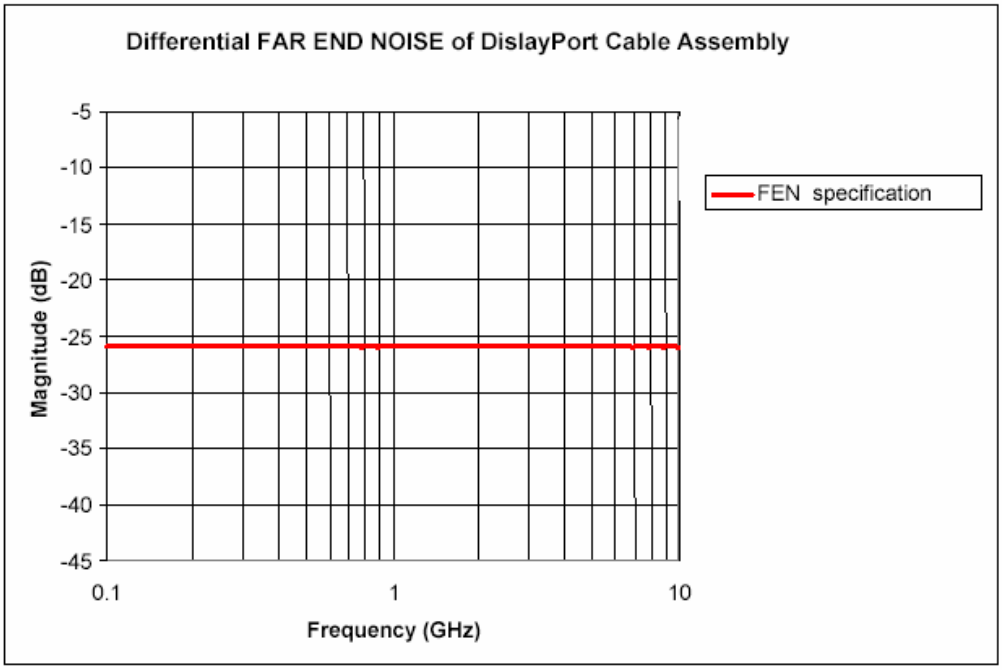



**Figure 4.7 Far End Total Noise (peak) for High-bit-rate Cable Assembly**

### *4.1.5.4 Intra-/Inter-pair Skew*

Both Intra-Pair and Inter-Pair skew are measured in the time domain with Differential TDR at fixture rise/fall time, i.e. 50ps measured (20% - 80%).

#### 4.1.5.4.1 Intra-Pair Skew

Intra-Pair skew shall be no more than 50ps and measured as depicted in Figure 4.8 below:

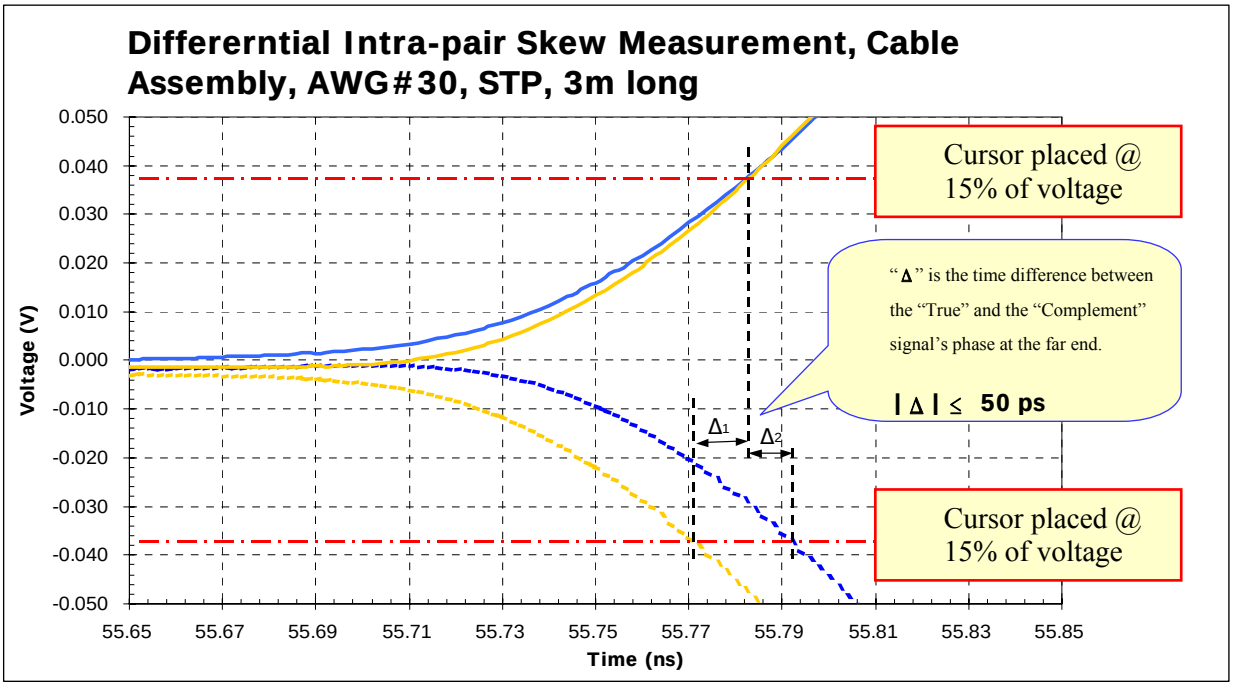



**Figure 4.8 Intra-Pair Skew Measurement Method**

#### 4.1.5.4.2 Inter-Pair Skew

Inter-Pair skew shall be no more than 200ps and measured as depicted in Figure 4.9 below:

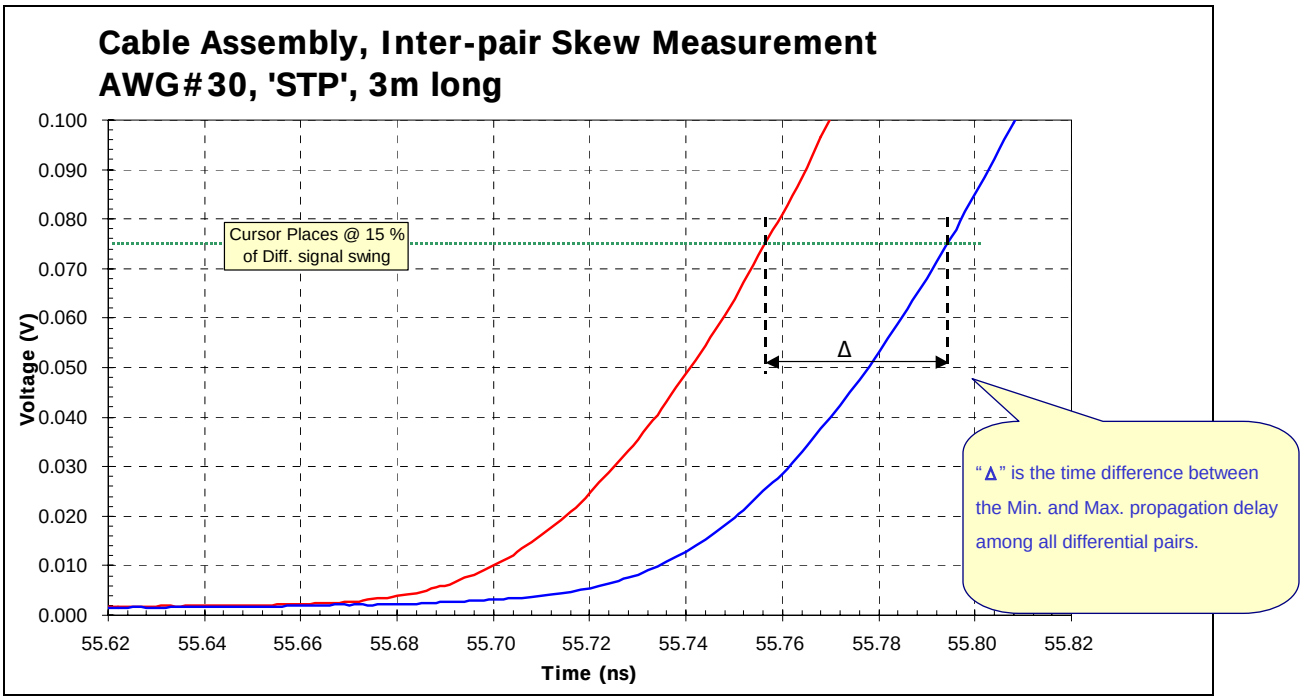



**Figure 4.9 Inter-Pair Skew Measurement Method**

## 4.1.6 Low-bit-rate Cable-Connector Assembly Specification

### *4.1.6.1 Insertion Loss & Return Loss*

The following equations represents the reference line that limits the 'Insertion Loss' and 'Return Loss' measured results.

#### 4.1.6.1.1 Insertion Loss Lower Limit for 15m Long, Cable Assembly:

$$IL_{\min.}[dB] = \begin{cases} -1 - 10 \times \sqrt{\frac{f}{f_0}} & ; \quad 0.01 < f \le \frac{f_0}{3} \\ -12 \times \left( \frac{3f - f_0}{3} \right) - 6.8 & ; \quad \frac{f_0}{3} < f \le 3 \end{cases}$$

Where:

$f$ is given in *GHz*

$f_0$ = 0.825 *GHz*

#### 4.1.6.1.2 Return Loss Upper Limit for 15m Long, Cable Assembly:

$$RL_{\max.}[dB] = \begin{cases} -20 & ; \quad f \le f_0 \\ -20 + 33\, Log_{10}\left( \frac{f}{f_0} \right) & ; \quad f_0 < f \le 2 f_0 \\ -10 + 12.56\, Log_{10}\left( \frac{f}{f_0} \times 0.5 \right) & ; \quad 2 f_0 < f \le 4 \end{cases}$$

Where:

$f$ is given in *GHz*

$f_0$ = 0.8 *GHz*

Figure 4.10 depicts the chart that represents the above mentioned equations 'Insertion Loss'. Figure 4.11 depicts the chart that represents 'Return Loss', and shall be referenced as the lower limit for 'Insertion Loss' and upper limit for 'Return Loss' respectively.

The cable assembly measured results shall comply with these limits.

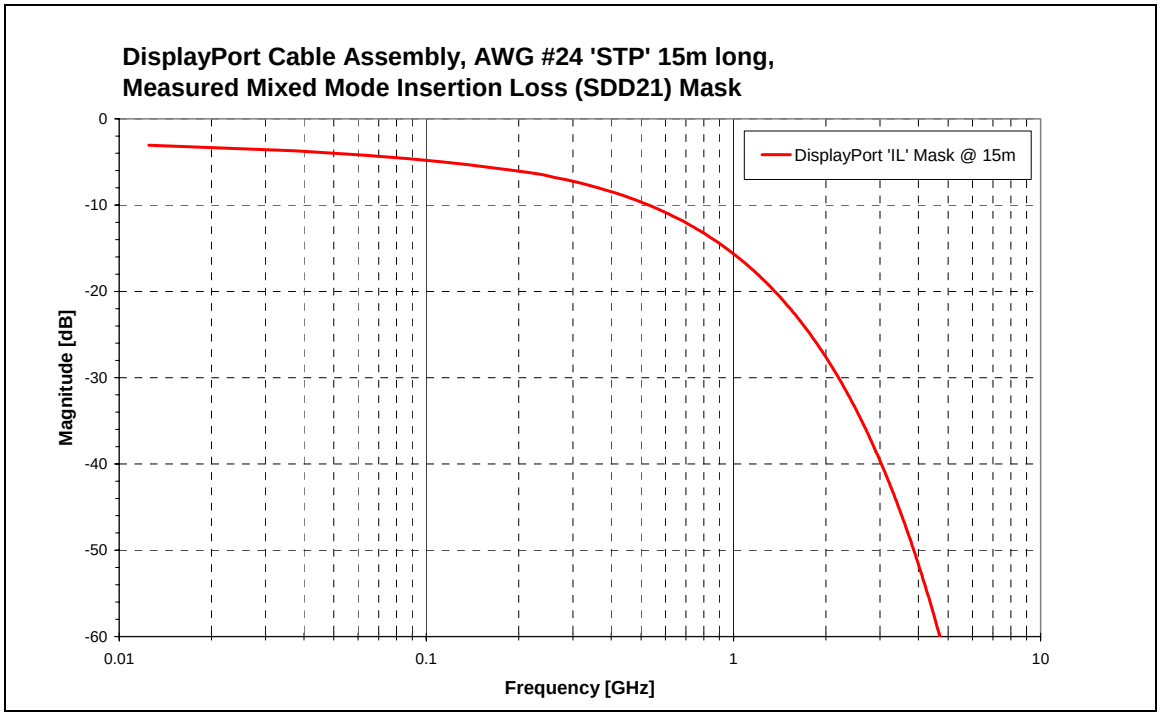



**Figure 4.10 Mixed Mode Differential Insertion Loss (SDD21)**

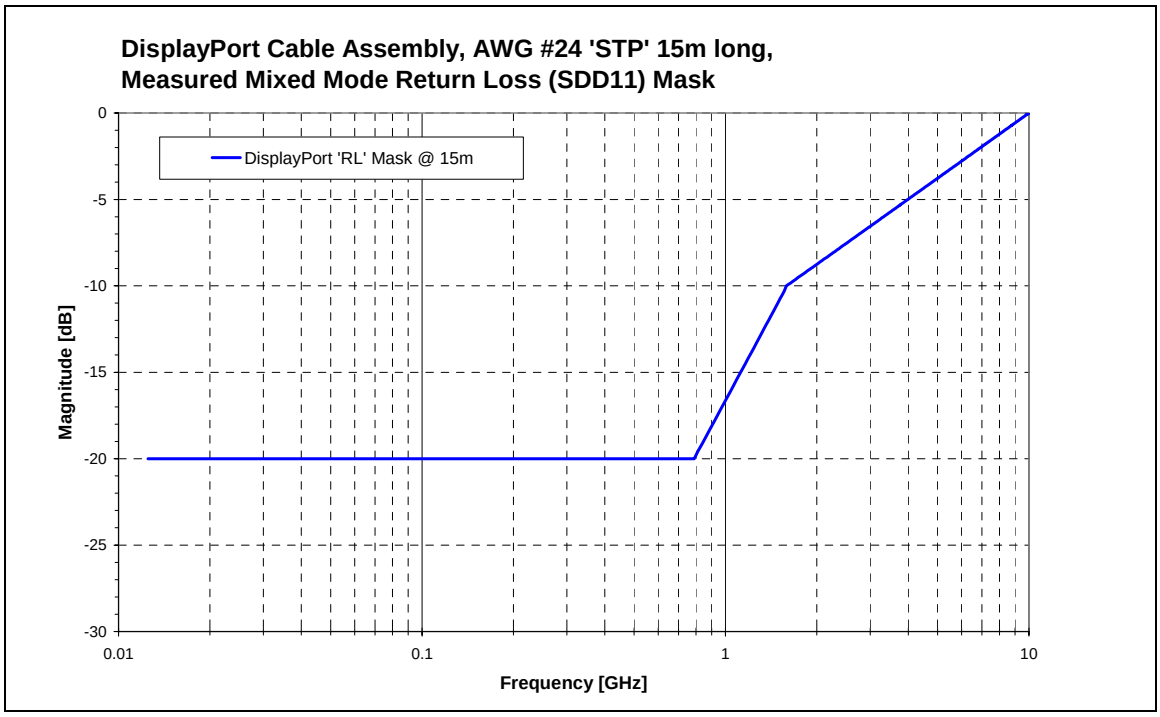



**Figure 4.11 Mixed Mode Differential Return Loss (SDD11)**

### *4.1.6.2 Near End Noise (NEN)*

Near End Noise shall be lower than the upper limit in the Isolation equation and depicted in Figure 4.12 below:

**Near End Noise - Upper Limit for 15m Long, Low Speed Cable Assembly:**

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 7 \end{cases}$$

Where:

$f$ is given in *GHz*

$f_0 = 0.8$ *GHz*

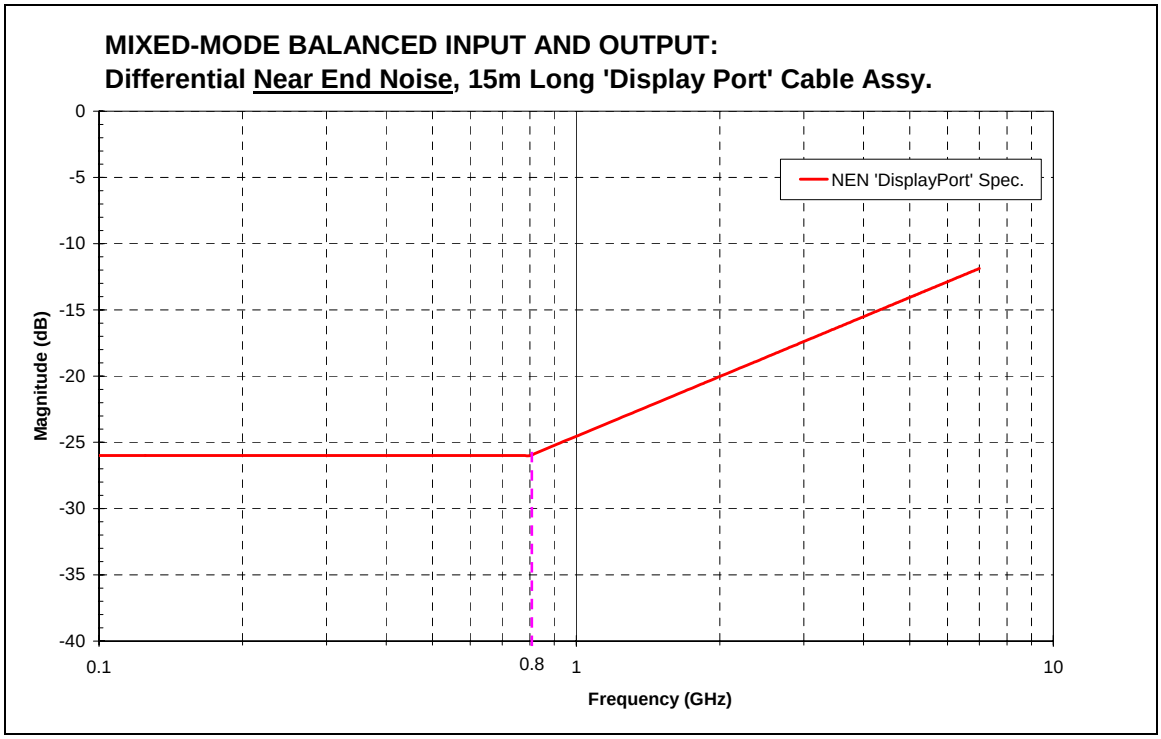



**Figure 4.12 Near End Total Noise (peak) for Low-bit-rate Cable Assembly**

### *4.1.6.3 Far End Noise (FEN)*

Far End Noise shall be lower than the upper limit depicted in Figure 4.13 below:

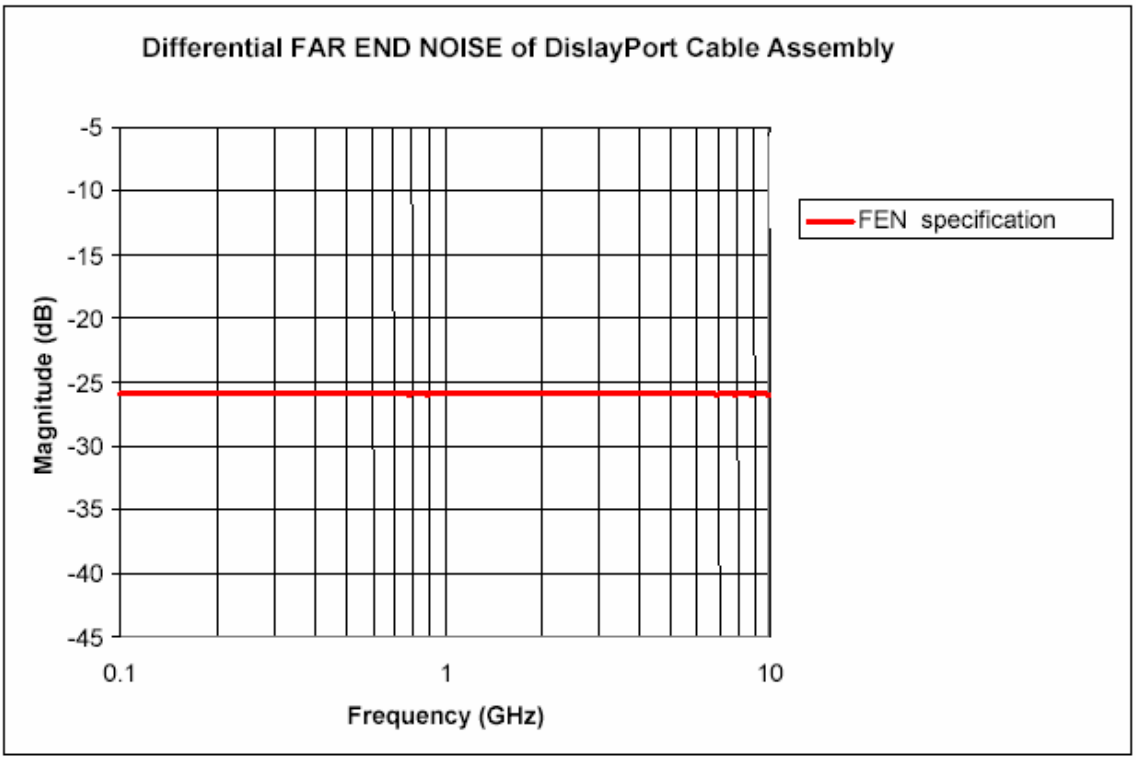



**Figure 4.13 Far End Total Noise (peak) for High-bit-rate Cable Assembly**

### *4.1.6.4 Intra-Pair Skew*

Intra-Pair is measured in the time domain with Differential TDR at fixture rise/fall time, i.e. 250ps measured (20% - 80%). Intra-Pair skew shall be no more than 250ps. As for the measurement method, refer to Figure 4.8 on p.163.

## 4.2 Connector Specification

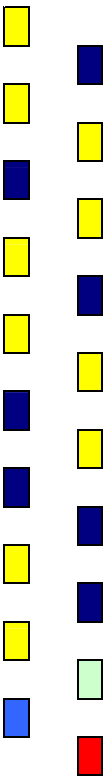
This section describes the specifications of the extenral and internal connectors of DisplayPort.

### 4.2.1 External connector

#### 4.2.1.1 Connector Pin Assignment

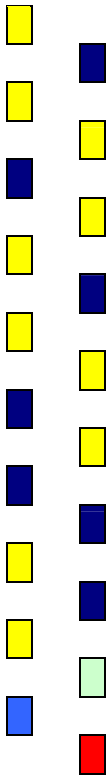
Table 4.3 and Table 4.4 show the pin assignments of the DisplayPort external connectors.

**Table 4.3 Source-Side Connector Pin Assignment**

| Pin Number | Signal Type | Pin Name | Mating Row Contact Location | Vertically Opposed Connector's Front View |
|---|---|---|---|---|
| 1 | Out | ML_Lane 0(p) | Top |  |
| 2 | GND | GND | Bottom | |
| 3 | Out | ML_Lane 0 (n) | Top | |
| 4 | Out | ML_Lane 1 (p) | Bottom | |
| 5 | GND | GND | Top | |
| 6 | Out | ML_Lane 1 (n) | Bottom | |
| 7 | Out | ML_Lane 2 (p) | Top | |
| 8 | GND | GND | Bottom | |
| 9 | Out | ML_Lane 2 (n) | Top | |
| 10 | Out | ML_Lane 3 (p) | Bottom | |
| 11 | GND | GND | Top | |
| 12 | Out | ML_Lane 3 (n) | Bottom | |
| 13 | GND | GND | Top | |
| 14 | GND | GND | Bottom | |
| 15 | I/O | AUX_CH (p) | Top | |
| 16 | GND | GND | Bottom | |
| 17 | I/O | AUX_CH (n) | Top | |
| 18 | In | Hot Plug Detect | Bottom | |
| 19 | PWR RTN | Return DP_PWR | Top | |
| 20 | PWR Out | DP_PWR | Bottom | |

**Note**: +5 - +12V power (with maximum current capacity of 500mA) from DP_PWR pin of DisplayPort Source Device may be used for powering DisplayPort Repeater Device or DisplayPort-to-Legacy converter within an active dongle. It is recommended that DisplayPort Sink Device and other Branch Devices have their own power and not depend on the DP_PWR over DisplayPort cable-connector assembly. The minimum power capacity provided by Source Device shall be 1.0W. Device with Sink Function that consumes more than 1.0W shall have its own power regardless of the device type.

**Table 4.4 Sink-Side Connector Pin Assignment**

| Pin Number | Signal Type | Pin Description | Mating Row Contact Location | Vertically Opposed Connector's Front View |
|---|---|---|---|---|
| 1 | In | ML_Lane 3(n) | Top |  |
| 2 | GND | GND | Bottom | |
| 3 | In | ML_Lane 3 (p) | Top | |
| 4 | In | ML_Lane 2 (n) | Bottom | |
| 5 | GND | GND | Top | |
| 6 | In | ML_Lane 2 (p) | Bottom | |
| 7 | In | ML_Lane 1 (n) | Top | |
| 8 | GND | GND | Bottom | |
| 9 | In | ML_Lane 1 (p) | Top | |
| 10 | In | ML_Lane 0 (n) | Bottom | |
| 11 | GND | GND | Top | |
| 12 | In | ML_Lane 0 (p) | Bottom | |
| 13 | GND | GND | Top | |
| 14 | GND | GND | Bottom | |
| 15 | I/O | AUX_CH (p) | Top | |
| 16 | GND | GND | Bottom | |
| 17 | I/O | AUX_CH (n) | Top | |
| 18 | Out | Hot Plug Detect | Bottom | |
| 19 | Power RTN | Return DP_PWR | Top | |
| 20 | Power In | DP_PWR | Bottom | |

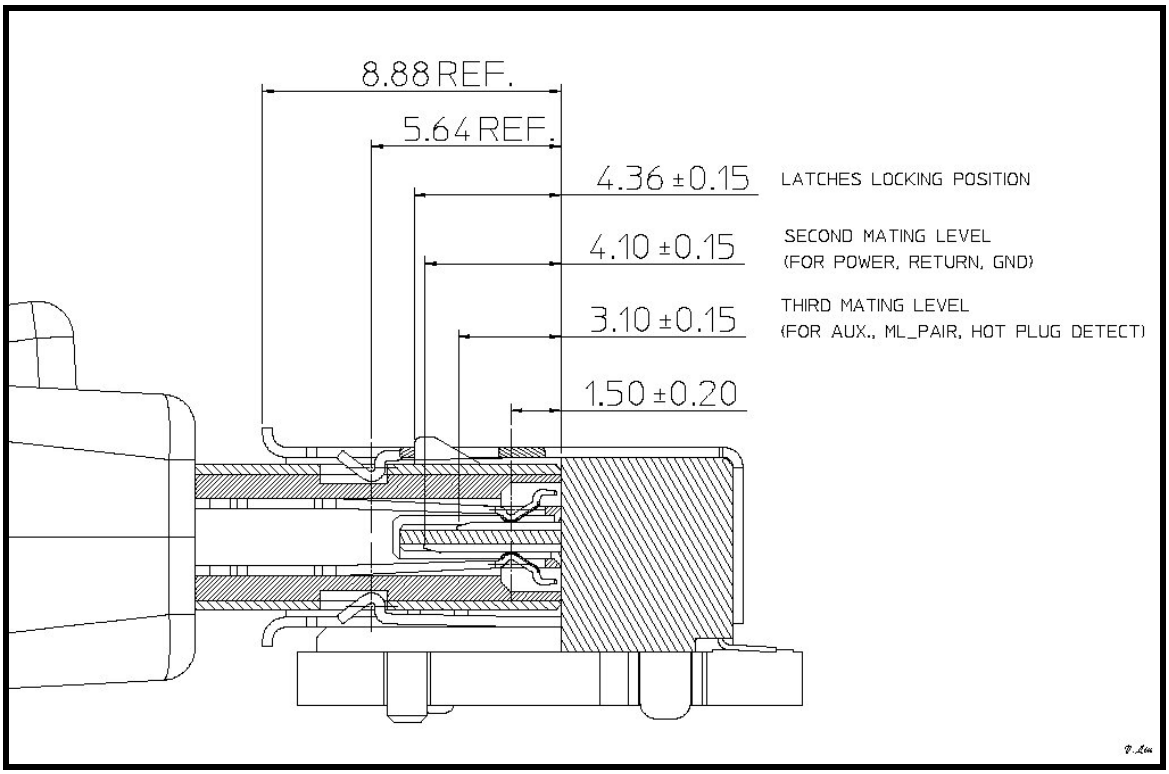
**Note**: +5 - +12V power (with maximum current capacity of 500mA) from DP_PWR pin of DisplayPort Source Device may be used for powering DisplayPort Repeater Device or DisplayPort-to-Legacy converter within an active dongle. It is recommended that DisplayPort Sink Device and other Branch Devices have their own power and not depend on the DP_PWR over DisplayPort cable-connector assembly. The minimum power capacity provided by Source Device shall be 1.0W. Device with Sink Function that consumes more than 1.0W shall have its own power regardless of the device type.

### *4.2.1.2 Contact Sequence*

Table 4.5 shows the legend for signal name/type mating level.

**Table 4.5 Mating Sequence Level**

| Signal Type | | | Level |
|---|---|---|---|
| Connector Shell | | | First Mate |
| DP_PWR | Return_DP_PWR | GND | Second Mate |
| Auxiliary (+)/(-) | ML_Lane (i) (+)/(-) | Hot Plug Detect | Third Mate |



### *4.2.1.3 Connector Mechanical Performance*

Table 4.6 below shows the mechanical performance of DisplayPort external connector.

**Table 4.6 Connector Mechanical Performance**

| Item | Test Condition | Requirement | |
|---|---|---|---|
| Vibration | Amplitude: 1.52mm P-P or 147m/s$^2$ {15G}<br><br>Sweep time: 50-2000-50Hz in 20 minutes.<br>Duration: 12 times in each of X, Y, Z axes (Total of 36 Times.<br>Electrical load: DC100mA current shall be flowed during the test.<br>(ANSI/EIA-364-28 Condition III Method 5A) | Appearance | No Damage |
| | | Contact Resistance | Contact:<br>Change from initial value:<br>30 mile-Ω maximum.<br>Shell Part:<br>Change from initial value:<br>50 mile-Ω maximum. |
| | | Discontinuity | 1μsec maximum. |
| Durability | Measure contact and shell resistance after the following.<br>Automatic cycling :<br>10,000 cycles at 100 ± 50 cycles per hour<br>(ANSI/EIA-364-09) | Contact Resistance | Contact :<br>Change from initial value:<br>30 mileΩ maximum.<br>Shell Part :<br>Change from initial value:<br>50 mileΩ maximum. |
| Insertion / Withdrawal Force (W/O latches) | Insertion and withdrawal speed : 25mm/minute.<br>(ANSI/EIA-364-13) | Withdrawal force | 9.8N {1.0kgf} minimum<br>39.2N {4.0kgf} maximum |
| | | Insertion force | 44.1N {4.5kgf} maximum |
| Latch Strength | Mate connectors, apply axial pull-out force in the axial direction at the speed rate of 13 mm/minute until the latch is disengaged or damaged.<br>(ANSI/EIA-364-98) | Appearance | No Damage on both connectors |
| | | Pull force | 49.0N {5.0kgf} minimum |
| Cable Flex | 100 cycles in each of 2 planes<br><br>Dimension:<br>X = 3.7 x Cable Diameter.<br>(ANSI/EIA-364-41, Condition I) | Discontinuity | 1 μsec maximum. |
| | | Dielectric Withstanding Voltage and Insulation Resistance | Conform to item of dielectric withstanding voltage and insulation resistance |

#### *4.2.1.4 Connector Electrical Performance*

Table 4.7 below shows the electrical performance of DisplayPort external connector.

**Table 4.7 Connector Electrical Performance**

| Item | Test Condition | Requirement |
|---|---|---|
| Low Level Contact Resistance | Mated connectors,<br>Contact: measured by dry circuit, 20 mVolts maximum, and 10mA.<br><br>Shell: measured by open circuit, 5 Volts maximum, 100mA. (ANSI/EIA-364-23) | Contact resistance excluding conductor resistance:<br>10 mile-Ω maximum.<br>(Reference requirement) |
| Dielectric Strength | Unmated connectors, apply 500 Volts AC (RMS.) between adjacent terminal and ground. (ANSI/EIA 364-20,Method 301)<br><br>Mated connector, apply 300 Volts AC (RMS.) between adjacent terminal and ground. | No Breakdown |
| Insulation Resistance | Unmated connectors, apply 500 Volts DC between adjacent terminal and ground. (ANSI/EIA 364-21,Method 302) | 100 mega-Ω minimum (unmated) |
| | Mated connectors, apply 150 Volts DC between adjacent terminal and ground. | 10 mega-Ω minimum (mated) |
| Contact Current Rating | 55 °C, maximum ambient<br>85 °C, maximum temperature change<br>(ANSI/EIA-364-70,TP-70) | 0.5 A minimum |
| Applied Voltage Rating | 40 Volts AC (RMS.) continuous maximum, on any signal pin with respect to the shield. | No Breakdown |
| Electrostatic Discharge | Test unmated connectors from 1 kVolt to 8 kVolts in 1 kVolt steps using 8mm ball probe. (IEC61000-4-2) | No evidence of Discharge to Contacts at 8 kVolts |

### *4.2.1.5 Connector Environment Performance*

Table 4.8 below shows the environment performance of DisplayPort external connector.

**Table 4.8 Connector Environment Performance**

| Item | Test Condition | Requirement | |
|---|---|---|---|
| Thermal Shock | 10 cycles of:<br>a) -55°Cfor 30 minutes<br>b) +85°C for 30 minutes<br>(ANSI/EIA-364-32, Condition I) | Appearance | No Damage |
| | | Contact Resistance | Contact:<br>Change from initial value:<br>30 mile-Ω maximum.<br><br>Shell Part:<br>Change from initial value:<br>50 mile-Ω maximum. |
| Humidity | A)<br>Mate connectors together and perform the test as follows.<br>Temperature : +25 to +85°C<br>Relative Humidity : 80 to 95%<br>Duration : 4 cycles (96 hours)<br>Upon completion of the test, specimens shall be conditioned at ambient room conditions for 24 hours, after which the specified measurements shall be performed.<br>(ANSI/EIA-364-31) | Appearance | No Damage |
| | | Contact Resistance | Contact:<br>Change from initial value:<br>30 mile-Ω maximum.<br><br>Shell Part:<br>Change from initial value:<br>50 mile-Ω maximum. |
| | B)<br>Unmate connectors and perform the test as follows.<br>Temperature : +25 to +85°C<br>Relative Humidity : 80 to 95%<br>Duration : 4 cycles (96 hours)<br>Upon completion of the test, specimens shall be conditioned at ambient room conditions for 24 hours, after which the specified measurements shall be performed.<br>(ANSI/EIA-364-31) | Appearance | No Damage |
| | | Dielectric Withstanding Voltage and Insulation Resistance | Conform to item of Dielectric Withstanding Voltage and Insulation Resistance |
| Thermal Aging | Mate connectors and expose to +105 ± 2°C for 250 hours. Upon completion of the exposure period, the test specimens shall be conditioned at ambient room conditions for 1 to 2 hours, after which the specified measurements shall be performed.<br>(ANSI/EIA-364-17, Condition 4, Method A) | Appearance | No Damage |
| | | Contact Resistance | Contact:<br>Change from initial value:<br>30 mile-Ω maximum.<br><br>Shell Part:<br>Change from initial value:<br>50 mile-Ω maximum. |

### *4.2.1.6 Connector Performance Test Sequence*

To evaluate the connector performance, the test sequence shall follow the test group 1, 2, 3 and 7 in the ANSI/EIA Standard (EIA-364-1000.01).

### *4.2.1.7 Connector Drawings ( Per Molex Connector P/N: 47272-0002)*

Figure 4.14 below shows the drawings of DisplayPort external connector. All dimensions are in mm.

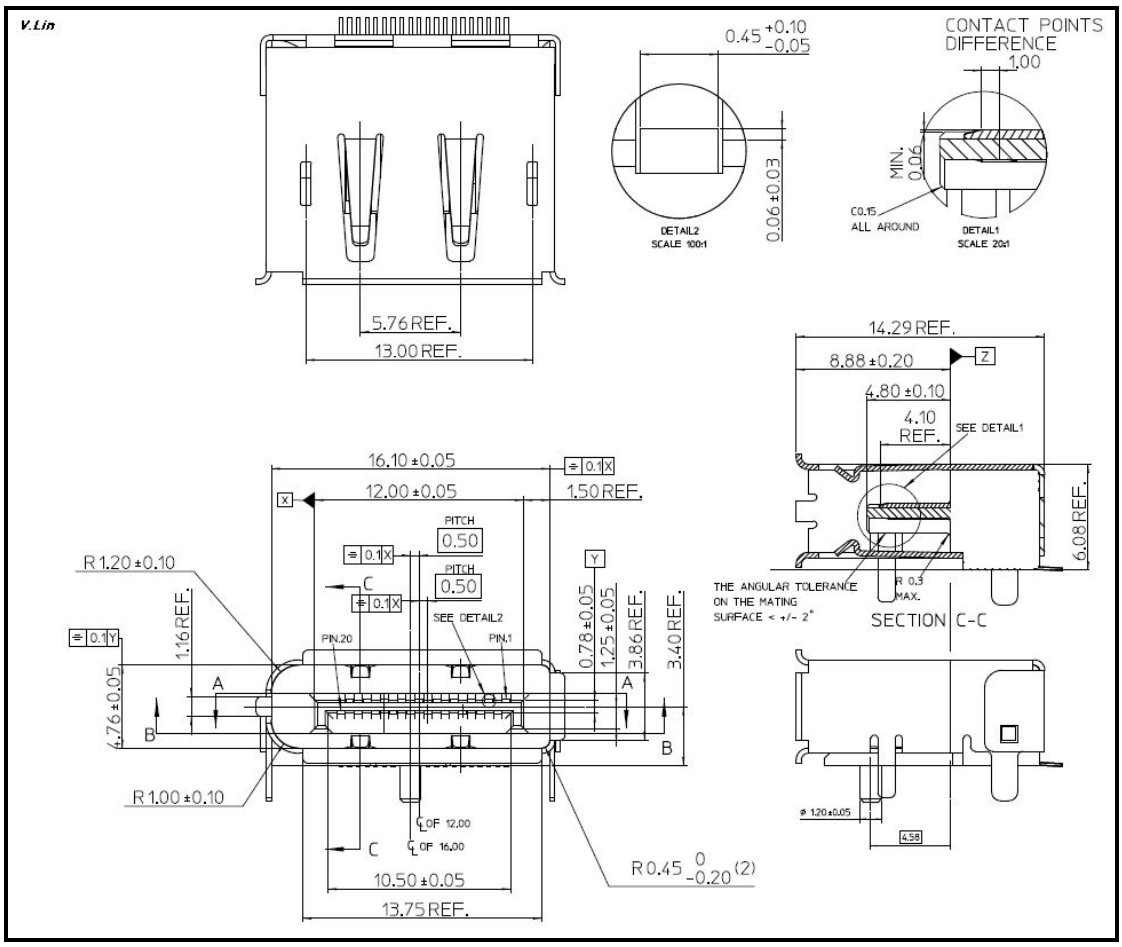



**Figure 4.14 DisplayPort External Connector Drawings**

### *4.2.1.8 Cable Connector Drawings (Per Molex Connector P/N: 47272-*001)*

Figure 4.15 below shows the drawings of DisplayPort external cable-connector assembly.

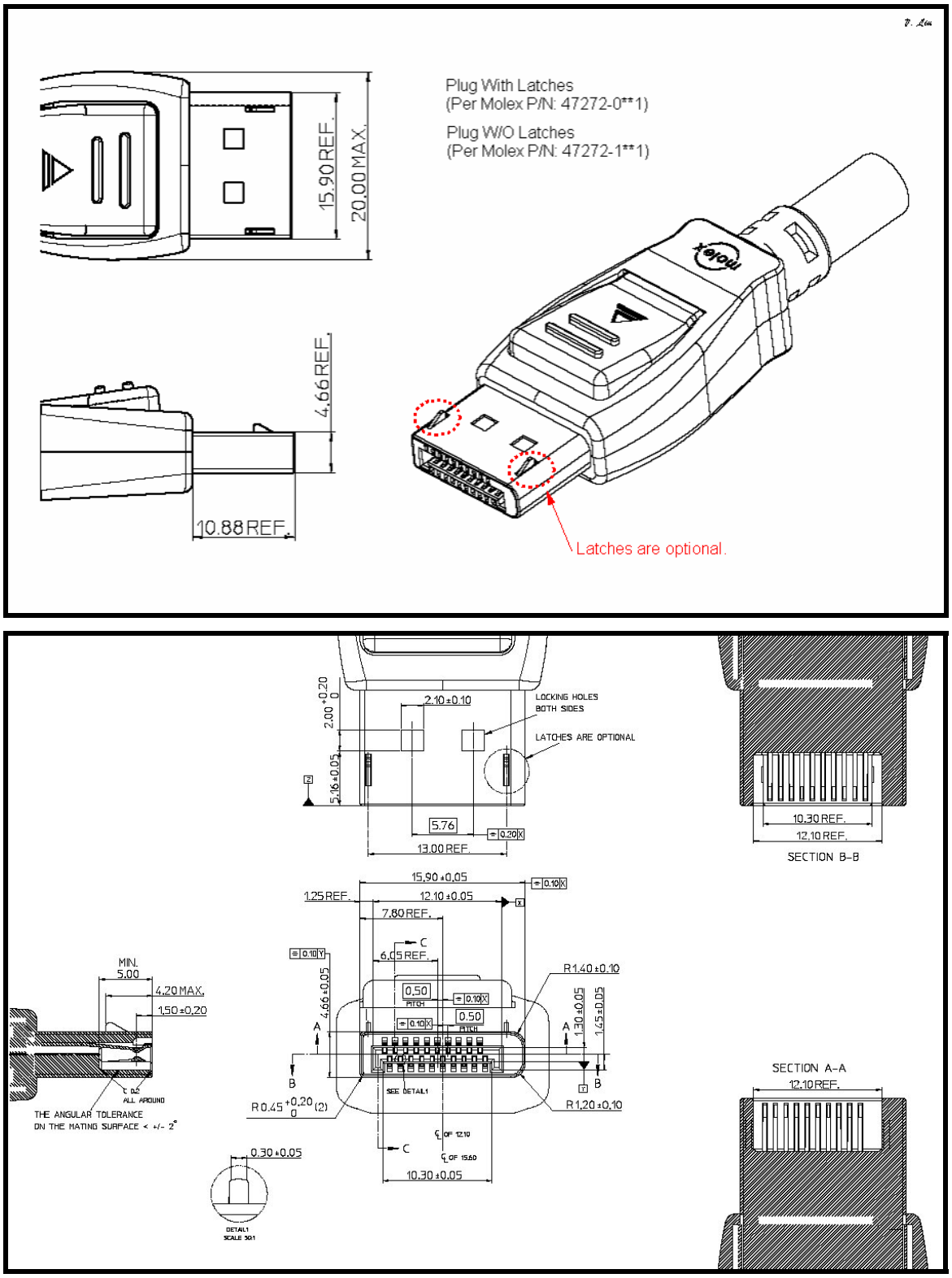



**Figure 4.15 DisplayPort External Cable-Connector Assembly Drawings**

#### *4.2.1.9 Plug connector and board connector fully mated condition*

Figure 4.16 below shows the fully mated condition of the plug connector and the board connector.

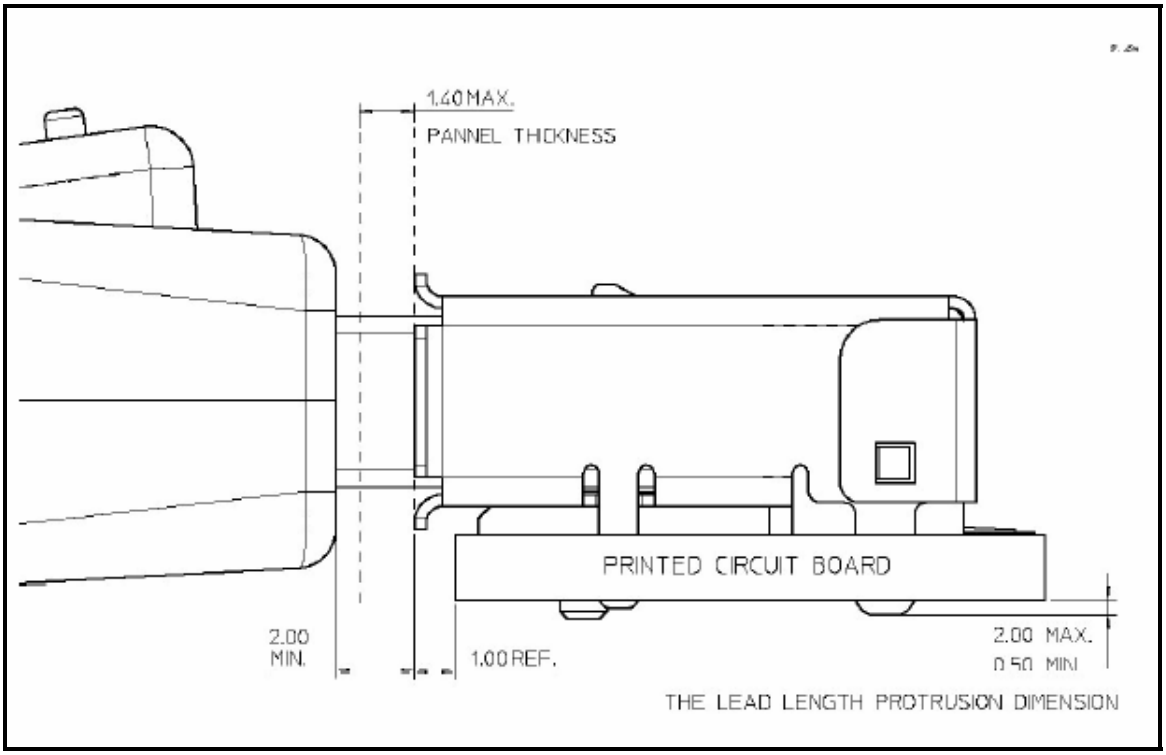



**Figure 4.16 Fully-mated Condition for DisplayPort External Connectors**

### *4.2.1.10 Recommended PCB Layout*

Figure 4.17 below shows the drawings of DisplayPort external cable-connector assembly.

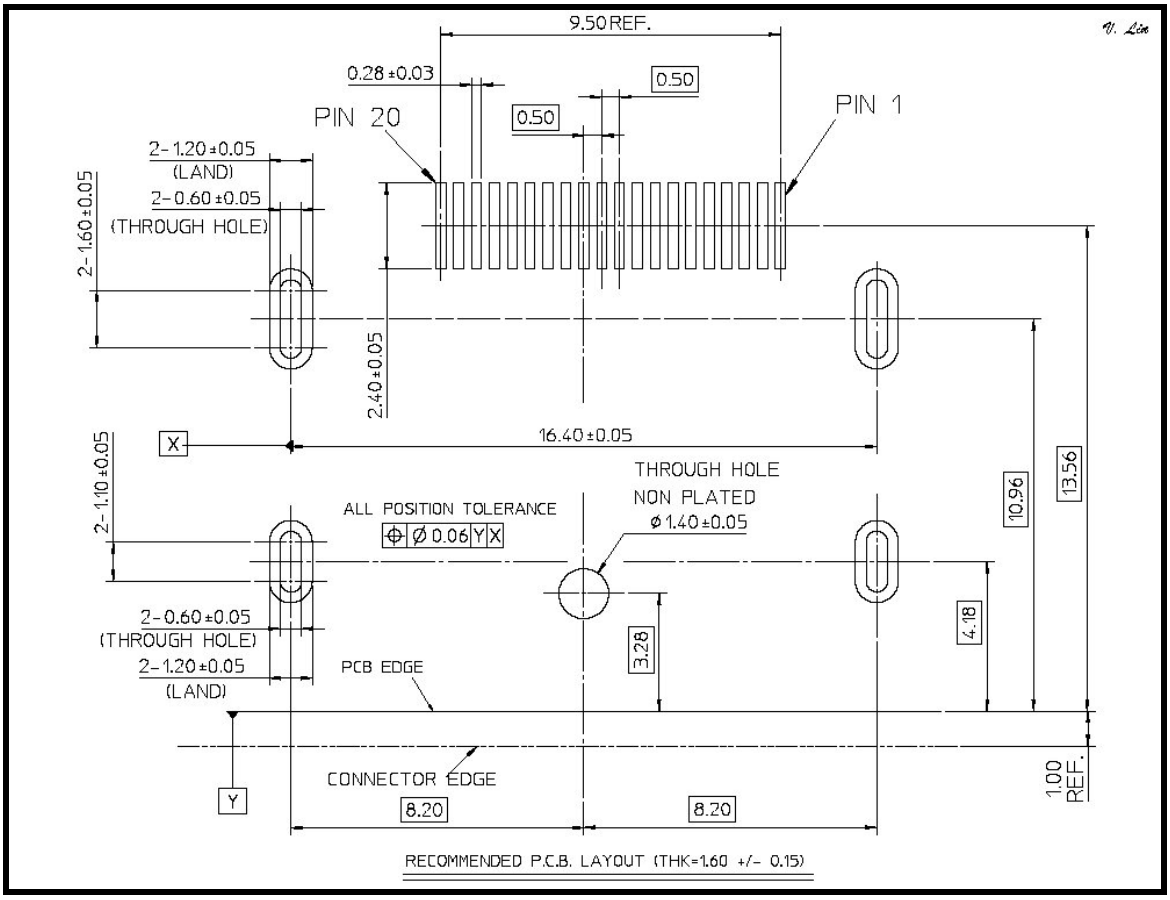



**Figure 4.17 Recommended PCB Layout for DisplayPort External Connector**

### *4.2.1.11 Reference Design for 4 DisplayPort External Connectors on STD PCI Card*

Figure 4.18 is a reference application design for the 4 external connectors on standard PCI card. Figure 4.19 shows the panel cut-out reference dimensions.

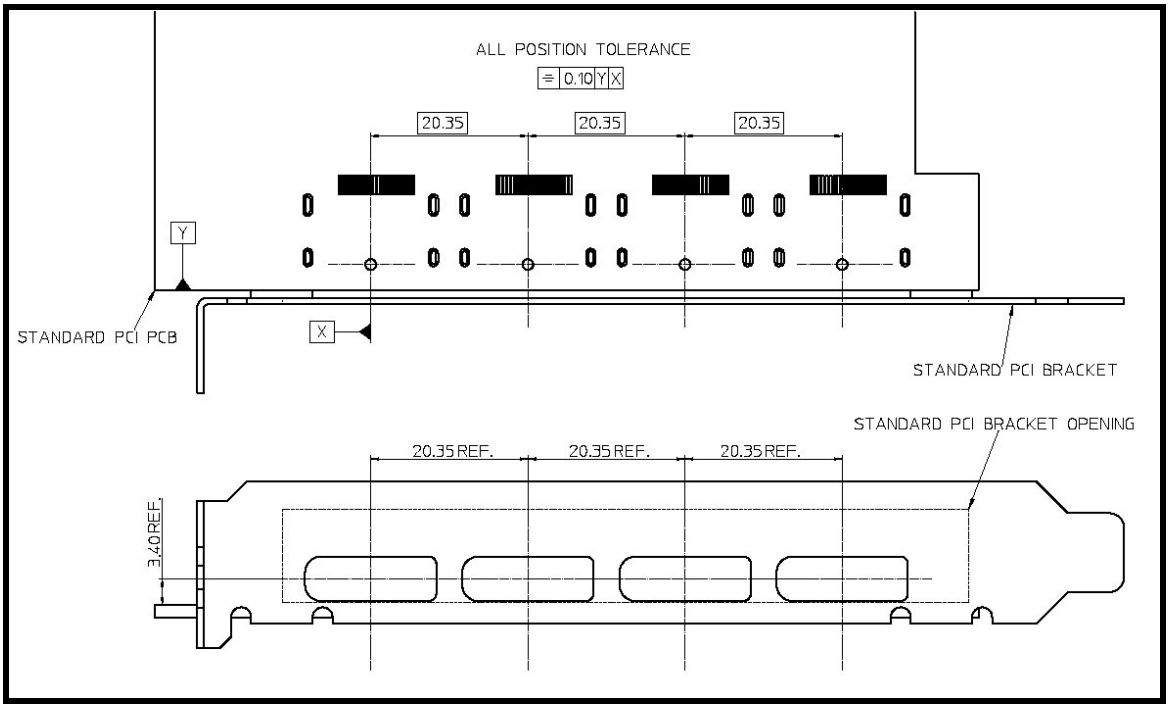



**Figure 4.18 Reference Design for 4 DisplayPort External Connectors on STD PCI Card**

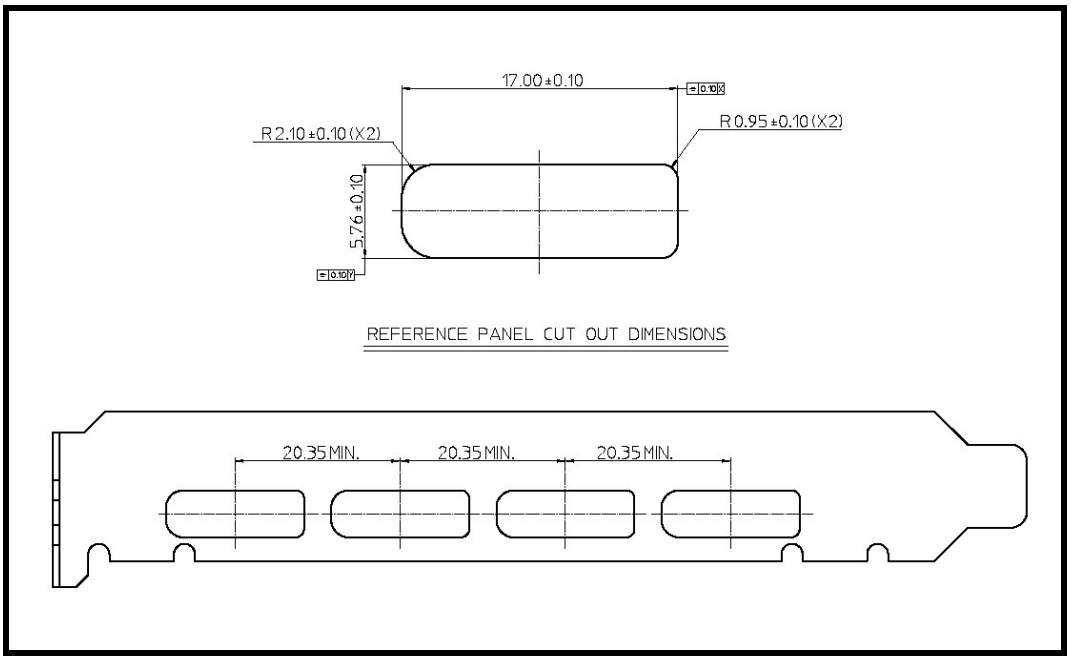



**Figure 4.19 Panel Cut Out Reference Dimensions**

### 4.2.2 Panel-side Internal Connector

This section covers the specifications for DispayPort panel-side internal connector.
The panel-side internal connectors consist of two-piece, 30-position, low profile, cable-to-board, co-planar connectors. One terminates the cable (Plug) and the other is attached to the PCB (Receptacle).

The connectors support up to four Main Link lanes (Lane 0 - Lane 3). In embedded connection, the cable connector assembly may support one, two, or four lanes depending on the bandwidth requirement of the application. For one-lane and two-lane Main Link configurations, the stuffing rule shall be as follows:

- When only two lanes are needed, Lane 0 and Lane 1 shall be populated while Lane 2 and Lane 3 are unpopulated.
- When only one lane is needed, Lane 0 shall be populated while Lane 1 - Lane 3 are unpopulated.

Only the panel TCON (timing controller) side of the connector is defined in this specification. While some cables may have the same connectors on both ends of the cable-connector assembly, others may have more pins for the Source Device side (that is, the side of graphics processor, LCD controller, etc.) for LCD backlight control, for instance.

### *4.2.2.1 Panel-side Internal Connector Pin Assignment*

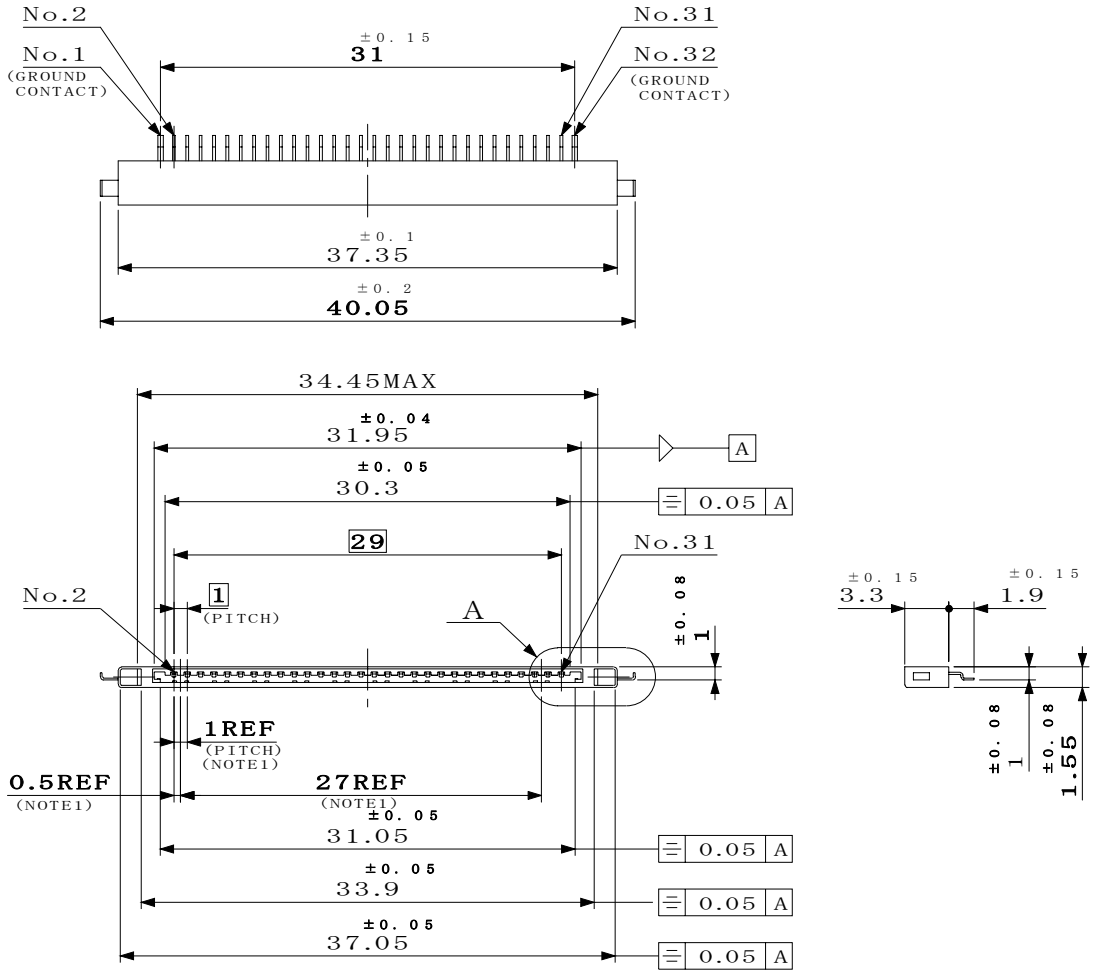
Table 4.9 below shows the pin assignment of DisplayPort panel-side internal connector.

**Table 4.9 DisplayPort Panel-side Internal Connector Pin Assingment**

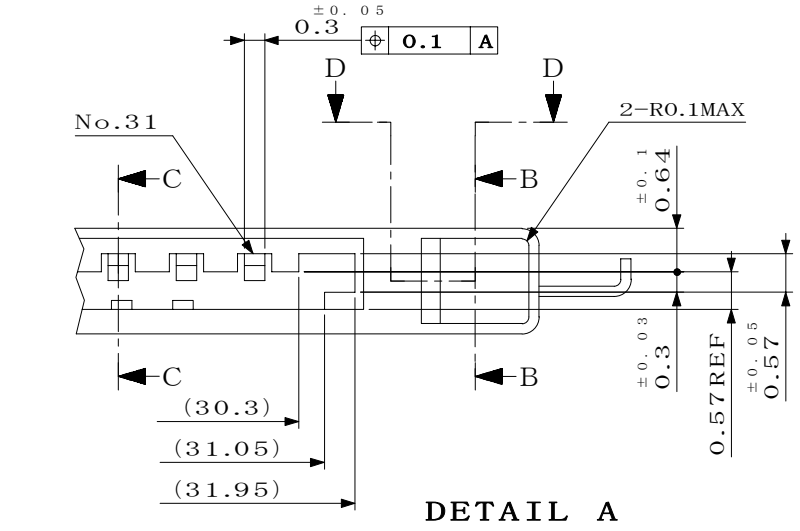
| Pin # | Pin Name | Pin Definition |
|---|---|---|
| 1 | | Optional (Outer shell connection-not a signal contact) |
| 2 | Reserved | |
| 3 | LCDVCC | Power to LCD panel. Controlled on graphics card and is removed when LCD is off. |
| 4 | LCDVCC | |
| 5 | LCDVCC | |
| 6 | LCDVCC | |
| 7 | GND | Power Return (Ground) |
| 8 | GND | |
| 9 | GND | |
| 10 | GND | |
| 11 | Hot Plug Detect | Hot Plug Detect |
| 12 | Reserved | |
| 13 | Reserved | |
| 14 | H_GND | High Speed (Main Link) Ground |
| 15 | ML_Lane 3(n) | 'True' Signal-Mail Link Lane 0 |
| 16 | ML_Lane 3(p) | 'Complement' Signal-Mail Link Lane 0 |
| 17 | H_GND | High Speed (Main Link) Ground |
| 18 | ML_Lane 2(n) | 'True' Signal-Mail Link Lane 0 |
| 19 | ML_Lane 2(p) | 'Complement' Signal-Mail Link Lane 0 |
| 20 | H_GND | High Speed (Main Link) Ground |
| 21 | ML_Lane 1(n) | 'True' Signal-Mail Link Lane 0 |
| 22 | ML_Lane 1(p) | 'Complement' Signal-Mail Link Lane 0 |
| 23 | H_GND | High Speed (Main Link) Ground |
| 24 | ML_Lane 0(n) | 'True' Signal-Mail Link Lane 0 |
| 25 | ML_Lane 0(p) | 'Complement' Signal-Mail Link Lane 0 |
| 26 | H_GND | High Speed (Main Link) Ground |
| 27 | AUX_CH (p) | 'True' Signal – Auxiliary channel |
| 28 | AUX_CH (n) | 'Complement' Signal – Auxiliary channel |
| 29 | H_GND | High Speed (Main Link) Ground |
| 30 | Reserved | |
| 31 | Reserved | |
| 32 | | Optional (Outer shell connection-not a signal contact) |

### *4.2.2.2 Panel-side Internal Receptacle Connector*

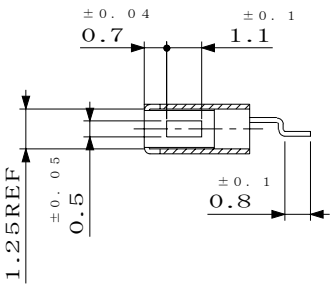
Figure 4.20 (which straddles two pages) and Figure 4.21 show the drawings of DisplayPort panel-side internal PCB receptacle connector and the recommended footprint layout, respectively.



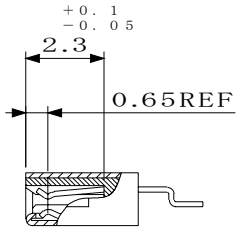

NOTE1.THIS DIMENSION SHOWS GROUND CONTACT



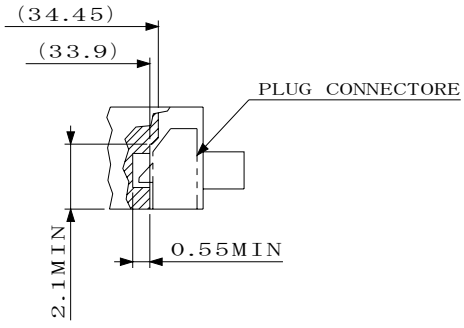

DETAIL A




SECT. B-B

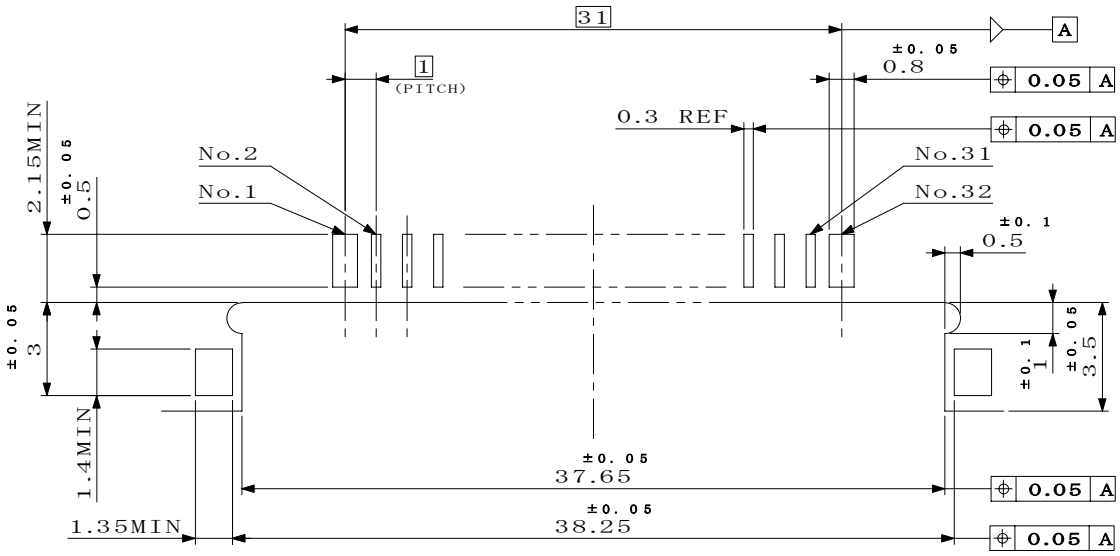



SECT. C-C




SECT. D-D

**Figure 4.20 Panel-side Internal PCB mount Receptacle Connector (in unit of mm)**

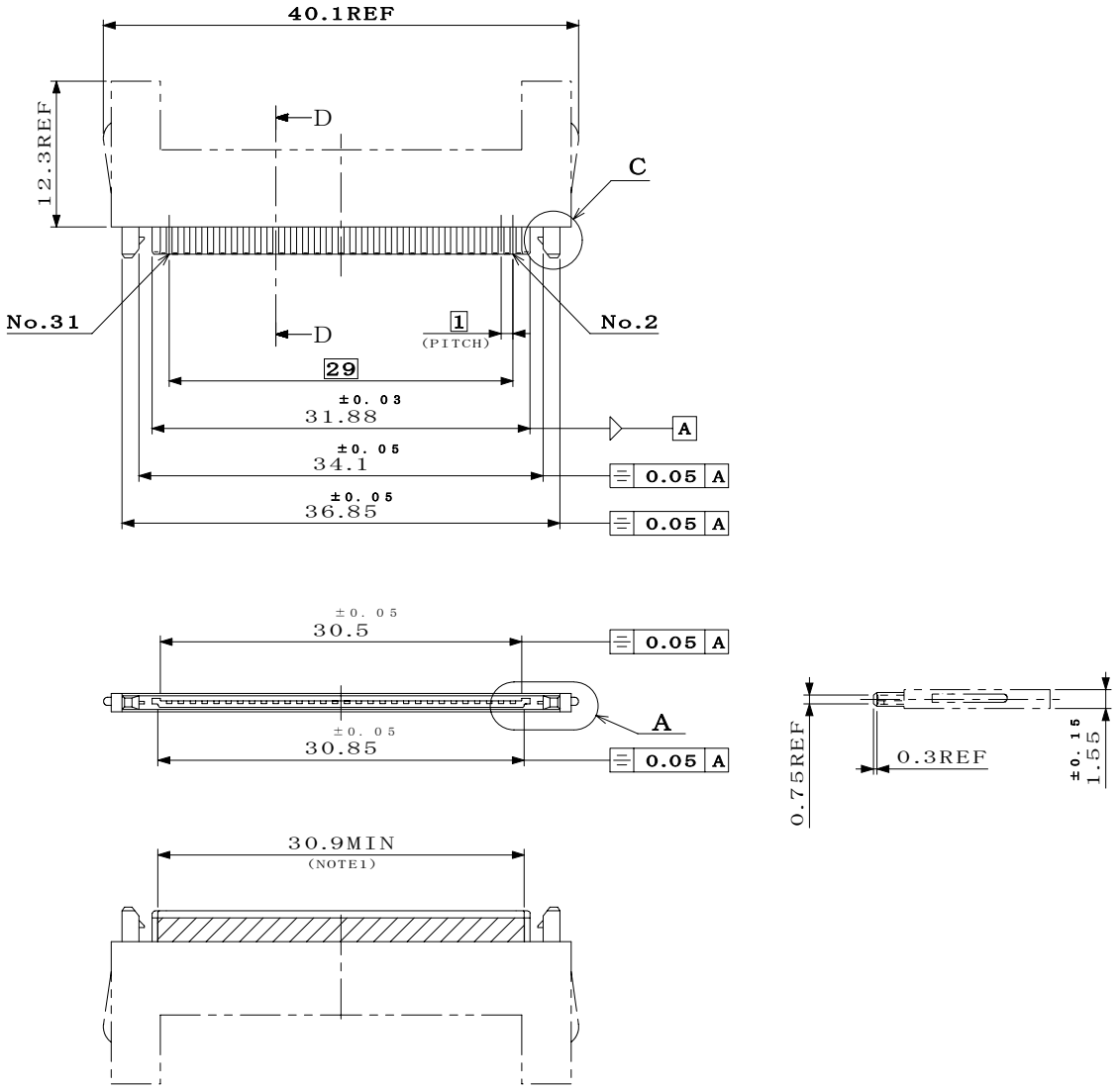



APPLICABLE P.C.B. DIMENSION(REF.)

**Figure 4.21 PCB mount Connector recommended footprint layout (in unit of mm)**

### *4.2.2.3 Panel-side Internal Plug Connector*

Figure 4.22 shows the drawings of DisplayPort panel-side internal cable plug connector.

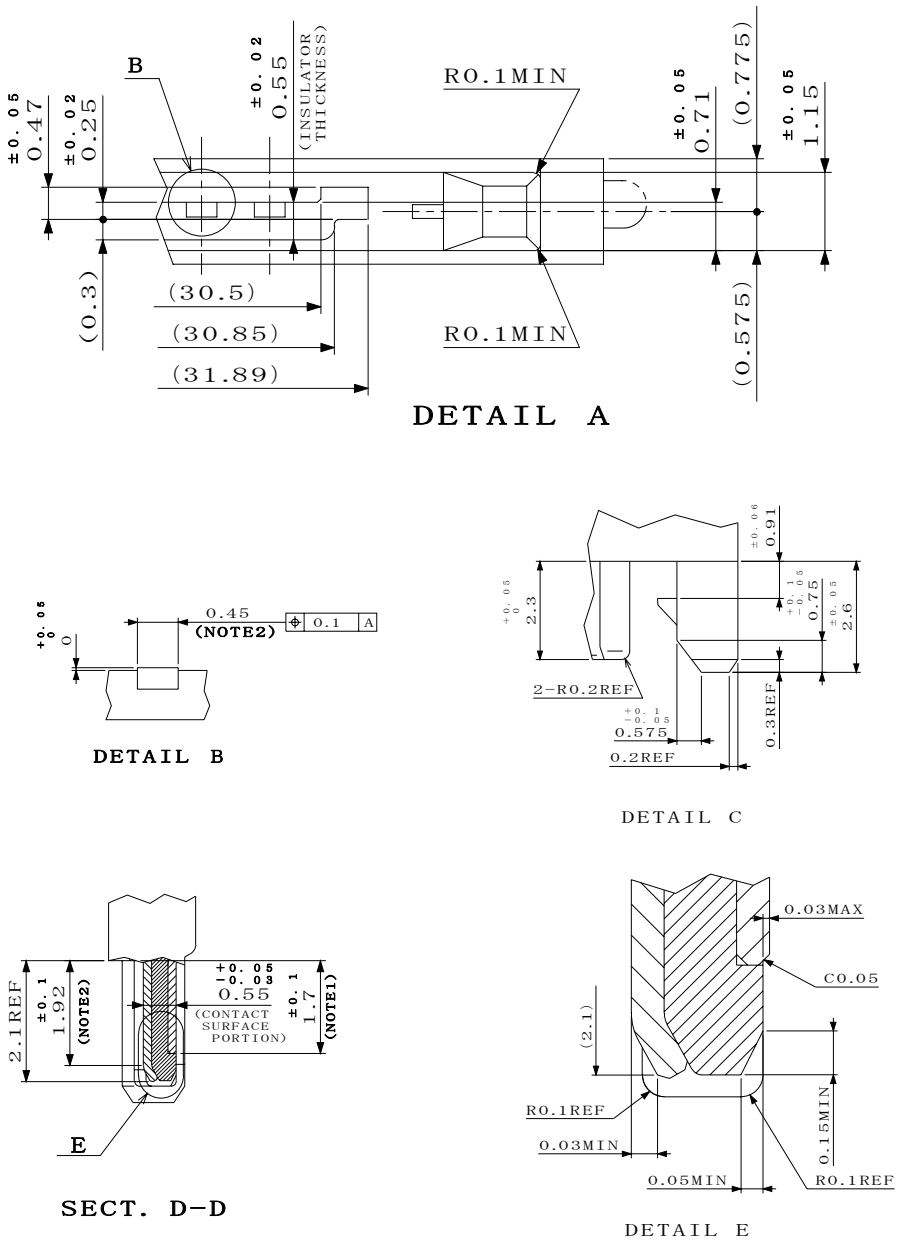



NOTE1.THIS AREA IS GROUND AREA

**Figure 4.22 Panel-side Internal Cable Plug Connector (in unit of mm)**

### *4.2.2.4 Panel-side Internal Plug Connector – Contact and Mechanical Guide Details*

Figure 4.23 and Figure 4.24 show the contact and mechanical guide details.




NOTE1.THIS AREA IS GROUND AREA
2.THIS AREA IS SIGNAL CONTACT AREA

**Figure 4.23 Contact and mechanical guide details (in unit of mm)**

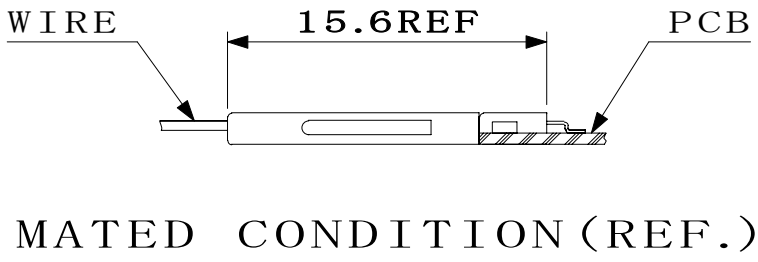



**Figure 4.24 Mating Condition (Reference) of panel side internal cable connector (in unit of mm)**

### *4.2.2.5 Panel Side Connector Mechanical Requirements*

Table 4.10 below shows the mechanical requirements of the panel-side connector.

**Table 4.10 Panel-side Connector Mechanical Requirements**

| ITEM | TEST CONDITION | REQUIREMENT |
|---|---|---|
| Vibration (Random) | Frequency: 10Hz to 2000Hz<br>Acceleration Vel. 30.38m/s$^2$ (3.1G) RMS.<br>Ation direction: In each of 3 mutually perpendicular planes.<br>Duration: 15 minutes each sample.<br>EIA-364-28, Test condition VII, test condition D. | 100mA applied with no electrical discontinuity greater than 1µ sec. |
| Physical Shock | Sample should be mounted on the test jig as mounted on the PCB.<br>Aceleration velocity 490m/s$^2$ or 50G.<br>Waveform: half sine<br>Duration:11 msec.<br>Number of drops: 3 drops each to normal and reversed directions of X,Y and Z axis. Total 18 drops.<br>EIA-364-27B method A | No electrical discontinuity greater than 1 µ sec. shall occur. |
| Durability (mating and unmating). | Number of cycles: 50<br>Automatic Cycling:<br>100 ± 50 cycles per hour<br><br>EIA364-09C | ΔR = 20mΩ Max. (Final) |
| Durabilty (preconditioning) | Number of cycles: 20<br>EIA-364-09C | No Physical Damage. |
| Connector Insertion Force | Operation speed :12.5mm/min<br>Measure the force required to mate connector including the latching mechanism.<br><br>EIA-364-13B | 25N (2.55kgf) Max. per connector |
| Connector Withdrawal Force | Operation speed :12.5mm/min<br>Measure the force required to unmate connector excluding the latching mechanism.<br><br>EIA-364-13B | 2.4N (0.245kgf) Max. per connector |
| | | |

### *4.2.2.6 Panel Side Connector Electrical Requirements*

Table 4.11 below shows the electrical requirements of the panel-side connector.

**Table 4.11 Panel-side Connector Electrical Requirements**

| ITEM | TEST CONDITION | REQUIREMENT |
|---|---|---|
| Dielectric withstanding voltage | 0.25 kVAC for 1 minute Test between adjacent circuits of unmated connectors. EIA364-20C | No creeping discharge or flashover shall occur. Current leakage : 0.5 mA Max. |
| Insulation Resistance | Impressed voltage 100 VDC Test between adjacent circuits of unmated connectors for 2 minutes. EIA-364-21C | 100 MΩ Min (initial) 50 MΩ Min. (final) |
| Low Level Contact Resistance | Subject mated contacts assembled in housing measured by dry circuit 20mV maximum open circuit at 10 mA (EIA-364-23B) | R = 30mΩ Max. (initial) ΔR = 20mΩ Max. (final) |
| Temperature Rise | Measure temperature rise by energizing current EIA-364-70A method 1 | 30ºC max. under loaded rated current. |
| | | |

### *4.2.2.7 Panel Side Connector Environmental Requirements*

Table 4.12 below shows the environmental requirements of the panel-side connector.

**Table 4.12 Panel-side Connector Electrical Requirements**

| ITEM | TEST CONDITION | REQUIREMENT |
|---|---|---|
| Humidity and Temperature Cycling | Cycle Mated connector,25ºC to 65ºC and 50% to 80% R.H. 10 cycles and 10 cycles of cold shock at -10ºC per EIA-364-31B method 4 | Mating Condition:<br>Contact Resistance:<br>R = 50mΩ Max. (final)<br><br>Unmating condition:<br>Insulation resistance (final)<br>50MΩ Min.<br>ΔR = 20MΩ Max. |
| Thermal Shock | Cycle mated connector from -55ºC for 30 minutes to 85ºC for 30 minutes repeat for 10 cycles. EIA-364-32 | ΔR = 20mΩ Max. (final) |
| Temperature Life (heat age) | Submit mated connector to 105ºC for 168 hours.<br>EIA-364-17B | ΔR = 20mΩ Max. (final) |
| Temperature Life (preconditioning) | Submit mated connector to 105ºC for 92 hours.<br>EIA-364-17B | No physical damage noted |
| | | |

# 5 Source/Sink Device Interoperability

This chapter describes the requirements for DisplayPort devices and cable-connector assemblies for the purpose of maximizing the interoperability between Source and Sink Devices over "Box-to-Box" DisplayPort link(s).

## *5.1 Source Device*

This section describes the requirement for Source Device for "Box-to-Box" connection. For embedded connection, it is the responsibility of a system integrator to ensure that the Source Device meet the requirement of a given application.

### 5.1.1 Stream Source Requirement

This subsection describes the requirements for the stream source in terms of video colorimetry, video timings, and audio formats.

#### *5.1.1.1 Video Colorimetry*

DisplayPort Source Devices shall support sourcing of both RGB and YCbCr colorimetry formats as shown in Table 5.1. Source Device shall indicate the colorimetry format (including the dynamic range) of the transmitted stream in the DisplayPort Main Stream Attributes as described in Section 2.2.4 on p.63.

In determining the colorimetry format, Source Device shall check the capability of Sink Device via EDID read. When the Sink Device capability is unknown, for example, due to corruption or absence of EDID, Source Device shall fall back to 18-bpp RGB, with full dynamic range (called "VESA range" as described in 5.1.1.1.1).

When Source device is transmitting RGB stream with a video timing format called out in CEA/EIA-861C Section 5 (except 640x480p) as using CEA range RGB, it shall use CEA range RGB. When a Source device is transmitting 640x480p 24 bit RGB, it will always use the full dynamic range.

**Table 5.1 DisplayPort Colorimetry Format Support**

| Colorimetry Format | Bit-depth per Pixel (bpp) | Bit-depth per Component (bpc) | Dynamic Range, Coefficients | Mandatory vs. Optional |
|---|---|---|---|---|
| RGB | 18 | 6 | "VESA range" only | Mandatory. Used in "fall-back" modes when Sink Device capability unknown. |
| | 24 | 8 | "VESA range" or "CEA range" | Mandatory. |
| | 30 | 10 | | Optional |
| | 36 | 12 | | |
| | 48 | 16 | | |
| YCbCr422 | 16 | 8 | "CEA range".<br><br>For CEA range, either 601 or 709 coefficients | Mandatory if YCbCr supported on any other display interface |
| | 20 | 10 | | Optional |
| | 24 | 12 | | |
| | 32 | 16 | | |
| YCbCr444 | 24 | 8 | | Mandatory if YCbCr supported on any other display interface |
| | 30 | 10 | | Optional |
| | 36 | 12 | | |
| | 48 | 16 | | |

**Note**: See the following sub-sections for definition of VESA range and CEA range.

#### 5.1.1.1.1 RGB Colorimetry

All the DisplayPort Source Devices shall support RGB colorimetry with pixel depth of 18, 24bpp. The 30, 36, 48 bpp RGB support is optional. As far as the RGB dynamic range is concerned, "VESA range" and "CEA range" are defined as follows:

- "VESA range" shall have:
  - Nominal zero intensity level at code value zero
  - Maximum intensity level at maximum code value allowed for bit depth, Namely, 63 for 18-bpp RGB, 255 for 24-bpp RGB, 1023 for 30-bpp RGB, 4095 for 36-bpp RGB, and 65,535 for 48-bpp RGB.
- "CEA range" shall have:
  - Nominal zero intensity level at 16 for 24-bpp, 64 for 30-bpp, 256 for 36-bpp, and 1024 for 48-bpp.
  - Maximum intensity level at maximum code value allowed for bit depth, namely, 235 for 24-bpp RGB, 940 for 30-bpp RGB, 3760 for 36-bpp RGB, and 60160 for 48-bpp RGB. Note that the RGB CEA range is defined for 24, 30, 36, 48 bpp RGB only, not for 18-bpp RGB.

When Source Device is transmitting RGB stream with a video timing format called out in CEA/EIA-861C Section 5 as using CEA range RGB, it shall use CEA range RGB.

However, Source Device may transmit all code values from zero to the maximum even when it declares the CEA range in the Main Stream Attributes. It is the responsibility of the Sink Device to limit the pixel value range as needed.

As noted earlier, Source Device falls back to 18-bpp, VESA range RGB when the Sink capability is unknown.

#### 5.1.1.1.2 YCbCr Colorimetry

Support for YCbCr colorimetry is required for DisplayPort Source Devices that support YCbCr or YPbPr on any other display interfaces.

Source Devices that support YCbCr shall support 24 bpp YCbCr 444 and 16 bpp YCbCr 422 in both 601 (defined in ITU-R BT.601-5 section 3.5 or EIA/CEA-770.2-C section 3.3) and 709 (defined by ITU-R BT.709-4 Part 1, Section 4 or EIA/CEA-770.3-C Sections 5.4 to 5.7) as the minimum.

In addition to the required minimum above, the pixel depth may optionally be 30, 36, 48 bpp for YCbCr444 and 20, 24, 32 bpp for YCbCr422.

YCbCr dynamic range is recommended to be as defined in CEA/EIA-861C Section 5 (CEA range):

- Y has nominal zero intensity level at 16 for 8 bits, 64 for 10 bits, 256 for 12 bits, 1024 for 16 bits per component
- Y has nominal maximum intensity level at 235 for 8 bits, 940 for 10 bits, 3760 for 12 bits, and 60160 for 16 bits per component
- Cb & Cr have their zero levels at 128 for 8 bit, 512 for 10 bit, 2048 for 12 bits, and 8192 for 16 bits per component
- Cb & Cr have nominal ranges of 16 to 240 for 8 bits, 64 to 960 for 10 bits, 256 to 3840 for 12 bits, and 1024 to 15360 for 16 bits per component.

However, Source Device may transmit all code values from zero to the maximum value. It is the responsibility of the Sink Device to limit the pixel value range as needed.

### *5.1.1.2 Video Timing Format*

In determining the video timing format, the stream source of Source Device shall check the capability of Sink Device via EDID read after Hot Plug Detect signal goes active. When Sink Device cannot handle the incoming stream, it shall toggle the HPD signal to notify Source Device of this condition. Upon detecting HPD pulse, Source Device shall find out the Sink Device status by reading SINK_STATUS byte of DPCD.

When the Sink Device capability is unknown, for example, due to corruption or absence of EDID, Source Device may fall back to a set of fall-back video timing formats its choice (except for the fail-safe mode). When none of the fall-back video timing formats is acceptable (as indicated by Sink Device via the SINK_STATUS bit), Source Device shall fall back to the fail-safe mode, which is 640x480 at 60Hz (as defined in VESA DMT standard).

### *5.1.1.3 Audio Format*

Audio support is optional for DisplayPort Source Devices. The Source Devices that support audio shall support stereo (2 channel) 16 bit per sample LPCM at one or more of 32 kHz, 44.1 kHz or 48 kHz. It is optional for the audio-capable Source Devices to support other sample rates, sample sizes or number of channels within the limits of the audio capability of the Sink Device indicated in its EDID.

Source Device shall check via EDID or the CEA Timing Extension to EDID what audio formats the Sink can support before sending any audio stream data.

As is the case with a video stream, Source Device is recommended to find out whether the Sink Device is able to sink the audio stream by checking SINK_STATUS bit of the Sink Device's DPCD and take corrective action as needed.

### 5.1.2 Source Device Link Configuration Requirement

Source Device shall support the number of Main Link lanes that provides for sufficient bandwidth even at a reduced bit rate per lane. For example, if a required application bandwidth is provided both with 2 lanes at a high bit rate and 4 lanes at a reduced bit rate, then the detachable Source Device is required to support 4 lanes.

Upon detecting IRQ Hot Plug Detect signal toggle, the Source Link Policy Maker shall read the Receiver Capability field of DPCD of the Sink Device and configures the link accordingly, using Link Training procedure as described in Section 2.5.3.3 on p.107 and Section 3.4.1.3 on p.128.

After the link is configured, the Source Link Policy Maker shall check the link status whenever it detects IRQ HPD pulse. When it detects that the link has lost lock, the Source Link Policy Maker shall re-train the link.

Upon detecting either DOWNSTREAM_PORT_STATUS_CHANGED bit of LANE_ALIGN__STATUS_UPDATED byte in DPCD set or low-going HPD pulse wider than 2 ms (Hot-plug-event HPD pulse), the Source Link Policy Maker shall re-read the Receiver Capability field of DPCD and take corrective action; For example, re-configure the link with reduced lane count, as needed.

Source Device changes the Main Link lane count during normal operation following the procedure below:

- Lane count increase
  - Stop the transmission of symbols over Main Link lanes.
  - Write the desired lane count to the link configuration field of DPCD via AUX CH.
  - Perform link training. Source may use the known-good drive current and pre-emphasis level setting to accelerate the link training sequence.
  - Once all the lanes are trained, start the transmission of Idle Pattern or a stream.
- Lane count reduction
  - Switch the transmitted symbols to Idle Pattern on all active lanes.
  - Write the desired lane count to the link configuration field of DPCP via AUX CH.
  - Stop the transmission of Idle Pattern over the lanes that are to be disabled.
  - Verify that DisplayPort receiver is symbol locked and inter-lane aligned (unless it is 1 lane configuration)
  - Start the transmission of a stream.

### 5.1.3 Source Device Behavior on Stream Timing Change

#### *5.1.3.1 Video Stream Timing Change*

Before changing the timing of the main video stream, Source Device shall transmit "idle pattern" (BS symbol followed by VB-ID with NoVideoStream_Flag and VerticalBlanking_Flag both set to 1 every $2^{13}$ or 8192 LS_Clk cycles) until it is ready to insert the new Main Stream Attribute data during the vertical blanking period of the main video stream. At the very minimum, Source Device shall repeat the idle pattern for 5 times before inserting the new Main Stream Attribute.

If Source Device chooses to stop the transmission of link symbols during the video timing change, it is required to run Link Training before starting the transport of the new main video stream.

Note that Source Device is allowed to continue transmitting Audio_Stream packet framed by SS and SE symbols, even when it is no longer transmitting the main video stream. When the video stream is absent for a prolonged period of time, Source Device shall transmit Audio_InfoFrame and Audio_TimeStamp packets after every 512$^{th}$ BS symbol set.

#### *5.1.3.2 Audio Stream Format/Timing Change*

As for audio format/timing change, Source Device shall set and keep VB-ID bit 2 (AudioMute_Flag) to 1 until after the new Audio InfoFrame and Audio_TimeStamp have been sent. Those packets may be sent as soon as the next frame boundary (when the main video stream is present) or after the next 512$^{th}$ BS symbol set (when the main video stream is absent).

### 5.1.4 Source Device Behavior upon HPD Pulse Detection

When there is a change either in link status (for example, loss of link synchronization) or device status (for example, remote control command pending), Sink Device generates low-going IRQ HPD pulse of 0.5ms - 1ms in duration.

Source Device shall check Link Status field of DPCD through AUX CH read to identify the cause within 100 ms after the rising edge of HPD signal. Source Device shall take corrective action once it has identified the cause.

The HPD pulse may be the result of a signal bounce upon cable-assembly unplugging. In this condition, AUX CH read operation is likely fail, and the HPD signal will eventually settle to low level for an extended period. Upon detecting HPD signal staying low for more than 100 ms, Source Device shall take corrective action for the Hot Unplug event. As for the action upon Hot Plug Detection, refer to Section 5.1.2.

## *5.2 Sink Device*

This section describes the requirements for Sink Device for "Box-to-Box" connection. For embedded connection, it is the responsibility of a system integrator to ensure that the Sink Device meet the requirement of a given application.

### 5.2.1 Stream Sink Requirement

This subsection describes the requirements for the stream sink in terms of video colorimetry, video timings, and audio formats. Sink Device shall describe its capabilities (supported Video Colorimetry Formats, Video Timing Formats and Audio Formats) in base EDID, the CEA-861 Timing Extension Block (optional).

#### *5.2.1.1 Video Colorimetry*

DisplayPort Sink Devices support sinking of both RGB and YCbCr colorimetry formats as shown in Table 5.1 on p.192. Sink Devices shall read the colorimetry format of the transmitted stream from the DisplayPort Main Stream Attributes.

When receiving CEA range video stream, Sink Device should anticipate that all the code values may be used by Source Device and clamp the dynamic range if needed.

#### *5.2.1.2 Video Timing Format*

DisplayPort Sink Device shall indicate whether it is able to sink the transmitted video stream by setting or clearing the SINK_STATUS bit of its DPCD.

All the detachable DisplayPort Sink Devices shall support 640x480 @60Hz as the fail-safe mode. Sink is not required to scale 640x480 to full screen or center the image, but all pixels are required to be visible.

#### *5.2.1.3 Audio Format*

DisplayPort Sink Device that outputs audio shall support audio input stream via DisplayPort link. The audio output may be sound waves (speakers) or electrical analog or digital audio output.

Sink Devices that support audio shall support stereo 16 bit LPCM at 32 kHz and 44.1 kHz and 48 kHz. It is optional for all the audio-capable Sink Devices to support other sample rates, sample sizes or number of channels.

Sink Device shall indicate via EDID or the CEA Timing Extension to EDID what audio formats it can support. As of this writing, only the CEA Timing Extension to EDID provides this information, but it is anticipated that future versions of VESA EDID may also specify audio capabilities of the Sink Device, and these would be acceptable to a DisplayPort Source Device.

As is the case with sinking video stream, Sink Device shall indicate whether it is able to sink the transmitted audio stream by setting or clearing the SINK_STATUS bit of its DPCD.

### 5.2.2 Sink Device Link Configuration Requirement

The Sink Device requirement for a supported link configuration depends on whether the device is a "lean-back" display or a "lean-in" display. A "lean-back" Sink Device is a display device that is meant to be viewed from more than 4 feet away.

A "lean-back" Sink Device shall support the number of Main Link lanes that provides for sufficient bandwidth even at a reduced bit rate per lane. This way, the lean-back display device can support a long cable length over which support of only a reduced bit rate is required.

Some of the examples of lean-back Sink Devices are TV displays and projectors. Table 5.2 and Table 5.3 show the examples of the required lane counts for those lean-back display devices.

**Table 5.2 Required lane count for typical TV timings at reduced bit rate**

| Timing | Lane Count | Remark |
|---|---|---|
| Up to 480p/576p @50-/60-Hz | One | |
| Up to 720p/1080i @50-/60-Hz | One @50Hz,<br>Two @60Hz | One @60Hz if 16-bpp YCbCr422 |
| Up to 1080p @50/60/Hz | Four | |

**Table 5.3 Required lane count for typical data projector timings at reduced bit rate**

| Timing | Lane Count | Remark |
|---|---|---|
| Up to 1024x768 (XGA) | One | 18-bpp |
| Up to 1680x1050 (WSXGA+), and 1600x1200 (UXGA) | Two | 18-bpp,<br>18-bpp, with reduced blanking |
| Up to 2048x1536 (QXGA) | Four | 18-bpp, with reduced blanking |

In the meantime, a lean-in display device such as a desktop monitor may choose to minimize the lane count for lowest cost. For example, 1400x1050 (SXGA+) desktop monitor may have only one Main Link lane. It should be noted that this SXGA+ monitor cannot receive a native input resolution over the one-lane, reduced-bit-rate link media.

A Sink Device with captive cable assembly is regarded as a lean-in device, and may choose to minimize the lane count.

## 5.2.3 Sink Device Behavior on Stream Timing Change

### *5.2.3.1 Main Video Stream Timing Change*

As described in Section 5.1.3, DisplayPort Source Device shall insert "idle pattern" (BS + VB-ID + Mvid7:0 +Maud7:0 with NoVideoStream_Flag and VerticalBlanking_Flag (bit 3 and bit 0) of VB-ID both set to 1 every $2^{13}$ or 8,192 LS_Clk cycles) at least 5 times before switching to a new video timing. Upon detecting this condition, Sink Device shall get ready to receive the new Main Stream Attribute and the main video stream data.

Whether to blank the display during this transition is implementation specific. Whatever method is taken, the visual glitch on the screen should be minimized.

### *5.2.3.2 Audio Stream Format/Timing Change*

As for audio format/timing change, Source Device shall set and keep VB-ID bit 2 (AudioMute_Flag) to 1 until after the new Audio InfoFrame and Audio_TimeStamp have been sent. Those packets may be sent

as soon as the next frame boundary (when the main video stream is present) or after the next 512th BS symbol set (when the main video stream is absent).

Sink Device shall mute the audio when AudioMute_Flag is set, and should be ready to receive a new audio format upon detecting the change in Audio InfoFrame and Audio_TimeStamp packets.

### 5.2.4 Toggling of HPD Signal for Status Change Notification

When there is a change either in link status (for example, loss of link synchronization) or device status (for example, remote control command pending), Sink Device shall clear the HPD signal to low for 0.5 ms - 1 ms before setting it to high again in order to notify Source device of status change.

## *5.3 Branch Device*

This section describes the requirement for DisplayPort Branch Devices. Branch Device types are summarized in Section 2.1.4 on p.29.

### 5.3.1 EDID Access Handling Requirement

Branch Device shall make sure that the stream transmitted by Source Device can be sunk by at least one Sink Device in the link. Therefore, Branch device without its own local Sink shall forward the EDID access from its upstream device to its downstream device.

When Branch Device has multiple downstream ports, it has multiple choices regarding which downstream device(s) to forward the EDID access to. This choice is implementation specific. One example is for such Branch Device to always choose a downstream device connected to Downstream Port 0.

### 5.3.2 Branch Device Link Configuration Requirements

DisplayPort repeaters (DisplayPort-in, DisplayPort-out) shall support four Main Link lanes both for receive port and downstream port. DisplayPort repeaters shall configure the downstream link the same way (in terms of lane count, bit rate per lane, and down spread) as the upstream link is configured. Once both the upstream and downstream links are configured, DisplayPort repeaters shall transport all DisplayPort control and data stream symbols from input to output. Table 5.4 below lists all the DPCD parameters Branch Device may update depending on the capability of its downstream links.

**Table 5.4 DPCD Parameters Branch Device May Update**

| DisplayPort Address | Parameters |
|---|---|
| 00000h | DPCD_REV<br>DPCD revision number<br>Bits3:0 = Minor Revision Number<br>Bits7:4 = Major Revision Number<br><br>10h for DPCD Rev.1.0<br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common revision number shall be used.* |
| 00001h | MAX_LINK_RATE<br>Bits4:0 = MAX_LINK_RATE<br>Maximum link rate of Main Link lanes<br>= Value x 0.27Gbps per lane<br><br>For DisplayPort Ver.1.0, only two values supported. All other values are reserved.<br>06h = 1.62Gbps per lane<br>0Ah = 2.7Gbps per lane<br><br>Bits7:5 = RESERVED. Read all 0's.<br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common link rate shall be used.* |
| 00002h | MAX_LANE_COUNT<br>Bits3:0 = MAX_LANE_COUNT<br>Maximum number of lanes = Value<br><br>For Rev.1.0, only the following three values are supported. All other values are reserved.<br>1h = One lane<br>2h = Two lane<br>4h = Four lanes<br><br>Bits7:4 = RESERVED. Read all 0's.<br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common lane count shall be used.* |
| 00003h | MAX_DOWNSPREAD<br>Bit 0 = MAX_DOWNSPREAD<br>0 – No spread supported<br>1 – 0.5% down spread<br><br>Bits7:1 = RESERVED. Read all 0's.<br>***Note**: Branch Device shall update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common down spread value shall be used.* |

Converters (either from DisplayPort to Legacy or from Legacy to DisplayPort) may have fewer than four Main Link lanes as long as DisplayPort link provides for the sufficient bandwidth for the Legacy link. The converters shall support the lane count that meets the bandwidth requirement at a reduced bit rate per lane.

#### *5.3.2.1 Behavior of Branch Device upon Downstream Status Change*

When Branch Device detects a change in its downstream link through Hot Plug/Unplug detection (for example, a Sink Device gets plugged to one of the downstream ports), it takes the following actions:

- If the downstream link is DisplayPort, read the DPCD Receiver Capability field of the connected downstream DisplayPort Receiver and update the DPCD Receiver Capability field (MAX_LINK_RATE, MAX_LANE_COUNT, etc.) to comprehend the capability of the downstream DisplayPort Receiver.
- Increase the SINK_COUNT value as follows:
  - If the immediate downstream link is DisplayPort, increase the SINK_COUNT value by the SINK_COUNT value of the immediate downstream device.
  - If the immediate downstream link is Legacy, increase the SINK_COUNT by 1 when the downstream link is detected "loaded."
    (**Note**: If the immediate downstream is Legacy without "loaded" detection, always assume the Sink is connected.)

Branch Device uses the HPD signal for communicating the status change of its downstream ports. Branch Device de-asserts HPD signal for 0.5 ms - 1 ms and re-asserts it. This resulting toggling of HPD signal shall be immediately detected by the upstream device. Link Policy Maker of the upstream device shall read the receiver capability field and link status field of DPCD after HPD signal goes high, and train the link when link has not been trained (as indicated in the link status field).

This process propagates upward until HPD toggling reaches the Source Device.

### *5.3.2.2 Example of Actions upon Addition of Sink Device (INFORMATIVE)*

Figure 5.1 shows an example of actions upon addition of Sink Device to DisplayPort link.

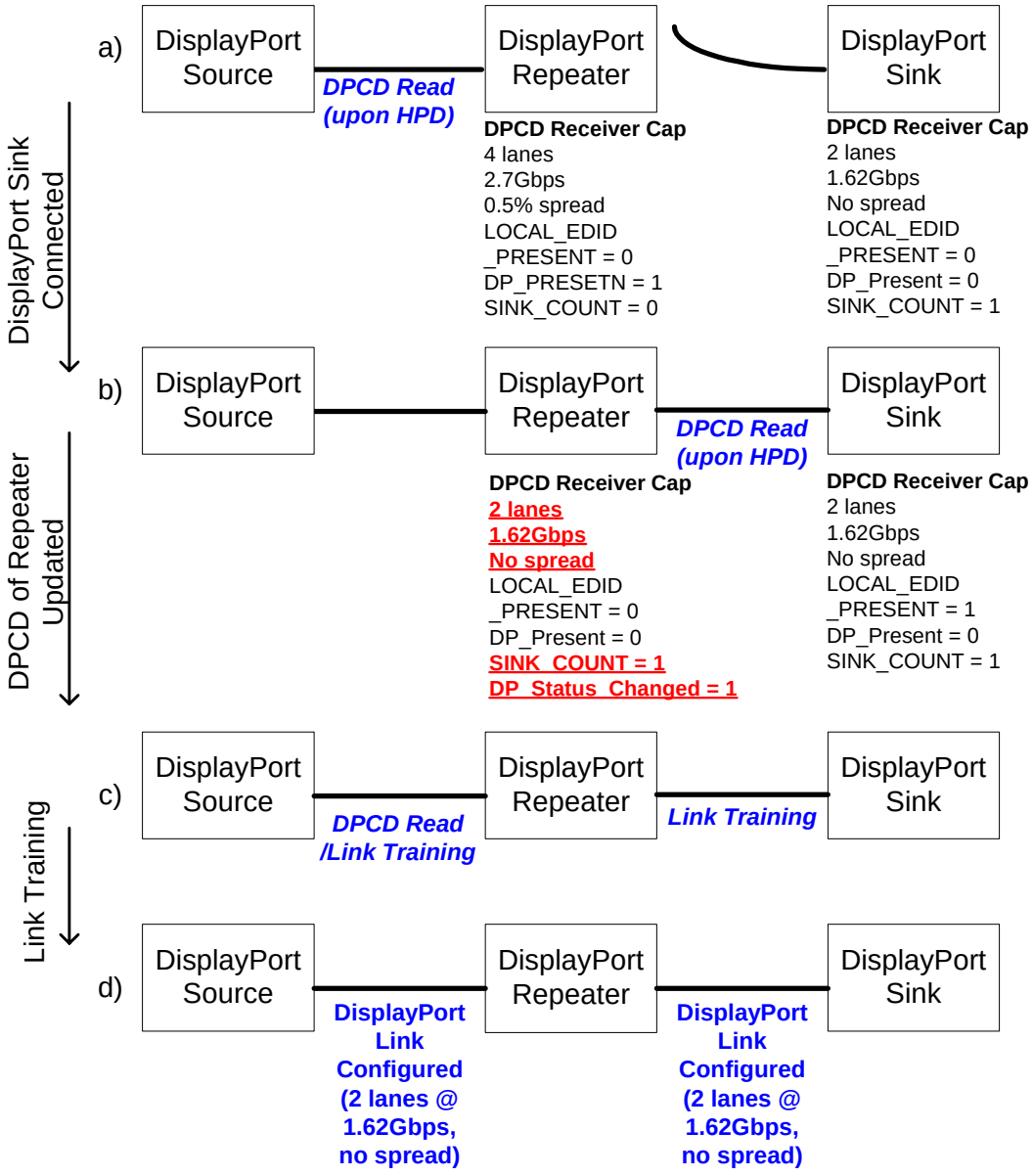



**Figure 5.1 Action Flow upon Addition of Sink Device**

## *5.4 Cable-Connector Assembly*

This section describes the requirement for the cable-connector assembly.

### 5.4.1 Box-to-Box, End-User-Detachable Cable Assembly

A box-to-box, detachable DisplayPort cable assembly shall support four Main Link lanes.

The box-to-box, detachable DisplayPort cable assemblies of 3 meters or shorter shall meet the high-bit-rate cable specification as specified in Section 4.1.4 on p.157. All of the box-to-box, detachable DisplayPort cable assemblies shall meet the low-bit-rate cable specification as specified in Section 4.1.6 on p.165.

The mating connectors of the box-to-box DisplayPort connection shall meet the connector specification as specified in Section 4.2 on p.169.

### 5.4.2 Embedded and Captive Cable Assembly

An embedded or captive DisplayPort cable assembly may support fewer than four Main Link lanes as long as "sufficient" link bandwidth is provided for a given application with fewer lanes. For embedded and captive connections, it is the responsibility of a system integrator to select the cable assembly with sufficient bandwidth capacity.

# APPENDIX 1 Link Layer Extension for DPCP Support

DPCP (DisplayPort Content Protection) is an optional feature of DisplayPort and its specification is separate from DisplayPort specification. This appendix briefly describes the Link Layer extension for supporting DPCP.

## *A1.1 DPCP Bulk Encryption/Decryption Blocks*

The bulk encryption sits at the end of the Link layer (just before the scrambler at the entry of the PHY Layer) while the bulk decryption sits at the beginning of Link Layer (just after the descrambler at the end of PHY Layer) as shown in Figure 2.8 on p.34 and Figure 2.9 on p.35, respectively. When the link is encrypted, all the information transmitted on the link is encrypted (pixel data, sea of dummy symbols, and secondary-data packets)

DPCP uses two additional control symbols, CPBS and CPSR. These symbols replace BS and SR respectively when DPCP is enabled.

When DPCP is on, "DPCP bulk encryption":

- Replaces BS with CPBS,
- Leaves any other control symbol untouched,
- Encrypts all data symbols, namely, valid main video stream data, sea of dummy symbols, and secondary-data packets.

When DPCP is off, "DPCP bulk encryption" leaves all symbols (control and data) untouched.

When DPCP is on, "DPCP bulk decryption":

- Replaces CPBS with BS,
- Leaves any other control symbol untouched,
- Decrypts all data symbols.

When DPCP is off, "DPCP bulk decryption" leaves all symbols (control and data) untouched.

DPCP alters the operation of the PHY Layer: it has to count both BS and CPBS symbols to replace every 512th of them with SR or CPSR, respectively in the transmitter. In the receiver, an SR or CPSR triggers a reset of the scrambler and is replaced with BS or CPBS, respectively.

## *A1.2 Support for CP Synchronization over the Link*

The content protection synchronization for DPCP is transported in a Secondary-data Packet. A new Secondary-data Packet Type Value 03h is used for DPCP (as shown in Table 2.33 on p.65),

The description of the content of the DPCP synchronization Secondary-data packet, with a maximum size of 32 bytes, is left to the DPCP specification. The synchronization data shall have sufficient redundancy on top of the ECC for Secondary-data packets described in Section 2.2.6 on p. 75.

When more than one lane is active, Secondary-data packets get split over the active lanes but this lane steering will be transparent to the DPCP specification.

Those synchronization packets are used to manage the cipher clock. Note that this clock is different from the link symbol clock.

### A1.3 AUX CH Transactions for DPCP

DPCP relies on the AUX CH for the content protection mutual-authentication and the content protection information transport. The AUX CH is also used to introduce a redundancy for the DPCP synchronization secondary-data packet in the Main Link.

The AUX CH is also used both to reset DPCP and to query the DPCP status information.

DPCP is managed at the link level. Within the DPCD address space for link services, address 70000h - 7FFFFh is reserved for DPCP. Furthermore, within the device service address space, 80000h - 807FFh is also reserved for DPCP.

For DPCP control, native command is used, instead of $I^2C$ mapping.