Video Electronics Standards Association

DisplayPort™ PHY Compliance Test Standard

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VESA DisplayPort™ PHY Compliance Test Standard

Version 1

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Purpose

The purpose of this document is to document the testing requirements for the DisplayPort Physical Layer to ensure interoperability.

Summary

This document details the test process specifics that, when followed, will enable high confidence that a DisplayPort product is an interoperable device. Test methods, test conditions, and test equipment requirements are expressed here as a means to completely define the high level interoperability test requirements.

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Revision History

September 14, 2007 Initial release of the standard

1 Overview

This DisplayPort PHY Compliance Test Standard establishes the superset test regimen for the determination of compliance of DisplayPort devices. It is segmented in Source, Receiver, Copper Cable, Hybrid Devices, and Tethered Devices.

This document is only intended to cover the DisplayPort PHY Layer. The Link Layer is covered by the DisplayPort Link Layer Compliance Test Standard.

It is important for the reader to know that if there is a conflict between this compliance test document and the DisplayPort Standard, the DisplayPort Standard statement shall be considered correct. In like manner, this document takes precedence over the Interoperability Guideline document.

The purpose of this document is to:

1. State the tests required for interoperability and the rationale for the tests.
2. Reference, where appropriate, the DisplayPort Standard.
3. State the high level requirements for each test with respect to device setup, test equipment, signal conditions, methodology and device to test instrument connectivity.
4. State the test limits for the measurement results.

Many tests are labeled as 'informative' and are viewed as being useful for characterization or debug purposes but are not necessarily significant in the determination of interoperability.

The compliance test specification is not intended to constrain test solution providers to a specific methodology or equipment set. Care has been taken to avoid specific vendors, methods or instrument types. All solution providers that address DisplayPort interoperability testing are expected to document their approach in meeting the requirements in each test. These documents are referred to as Methods of Implementation (MOI). MOI documents are controlled and submitted by each test provider and detail instrumentation, measurement steps, and other pertinent information regarding the process of acquiring the result required for the test.

1.1 Glossary/Acronyms

Table 1-1: Glossary

Terminology	Definition
Aggressor	A signal imposed on a system (i.e. cable assembly) for the purpose of measuring response on other signal carriers.
AUX CH	Half-duplex, bi-directional channel between DisplayPort transmitter and DisplayPort receiver. Consists of one differential pair transporting self-clocked data. The DisplayPort AUX CH supports a bandwidth of 1Mbps over DisplayPort link. DisplayPort Source is the master (also referred to as AUX CH Requester) that initiates an AUX CH transaction. DisplayPort Sink is the slave (also referred to as AUX CH Replier) that replies to the AUX CH transaction initiated by the Requester.
Box-to-box connection	DisplayPort link between two boxes detachable by an end user. A DisplayPort cable-connector assembly for the box-to-box connection shall have four Main Link lanes.
DisplayPort receiver	Circuitry that receives the incoming DisplayPort Main Link data. Also contains the transceiver circuit for AUX CH. Located in Sink Device and the upstream port of Intermediate Device.
DisplayPort transmitter	Circuitry that transmits the DisplayPort Main Link data. Also contains the transceiver circuit for AUX CH. Located in Source Device and in the downstream port of Intermediate Device.
Dual-standard Device	Source or Sink Device that supports both DisplayPort and DVI/HDMI operating modes.
HPD	Hot Plug Detect
Hybrid Device	A Hybrid Device is any device other than a copper cable that transports DisplayPort signals from a source to a sink
Informative	The designation of a test that is not required for compliance but is considered important from a characterization standpoint. It is provided for informational purposes only.
Main Link	Uni-directional channel for isochronous stream transport from DisplayPort Source to DisplayPort Sink. Consists of one, 2, or 4 lanes, or differential pairs. Supports 2 bit rates: 2.7Gb/s per lane (referred to as “High Bit Rate”) and 1.62Gb/s per lane (referred to as “Reduced Bit Rate”).
Normative	The designation of a test that is required for compliance.
Sink Device	A device that contains A/V stream sinks for display and/or sound.
Source Device	A device that contains a stream source and originates an isochronous A/V stream.
Test Access Fixture	A specialized assembly made to interface to a DisplayPort receptacle or plug and to allow access of signals for measurement or stimulation
Tethered Device	A Tethered Device is a source or sink that has as part of the product, a captive cable.
Type D Hybrid Device	A Hybrid device designed to connect directly to a sink device
Type T Hybrid Device	A Hybrid device designed to connect to a tethered cable of a sink device
Victim	A lane targeted for analysis for response to another active lane or signal source

Table 1-2: Acronyms

Acronyms	Abbreviated Terms
BER	Bit Error Ratio
BW	Bandwidth
DJ	Deterministic Jitter
DPCD	DisplayPort Configuration Data
DUT	Device Under Test
FEN	Far End Noise
Gb/s	Giga-bit per second
GHz	Giga Hertz $1x10^9$ cycles per second
HBR	High Bit Rate. 2.7Gb/s
IC	Illegal character
ISI	Inter Symbol Interference- degree that previous bit pattern affects subsequent edges
MHz	Mega Hertz $1x10^6$ cycles per second
MOI	Method of Implementation. Document that describes the test steps and methods taken in a specific test solution implementation.
mUI	milli-Unit Interval
mV	milli-volts
NEN	Near End Noise
PLL	Phase Locked Loop
PRBS	Pseudo random bit sequence. PRBS7 is sequence with 7^{th} order polynomial.
ps	picoseconds
RBR	Reduced Bit Rate. 1.62 Gb/s
RD	Running Disparity
SJ	Sinusoidal Jitter- jitter component that is sinusoidal in nature and exhibits a U-shaped distribution when plotted as a histogram
SSC	Spread Spectrum Clocking
SSG	Stressed Signal Generator
TJ	Total Jitter- The peak to peak jitter that supports a given bit error ratio
UI	Unit Interval. The reciprocal of the bit rate. At 2.7Gb/s, the UI=370.4ps. At 1.62Gb/s, the UI=617ps.
ζ	Zeta. Second order term a control system equation that determines degree of peaking

1.2 Reference Documents

Table 1-3: Reference Documents

Document	Version/revision	Date
VESA DisplayPort Standard	Version 1.1	March 19, 2007

All references to the DisplayPort Standard in this document refer to version noted in the above table.

2 Test Process Requirements

This section captures requirements for effective execution of the test processes identified in Sections 3, 4 and 5.

2.1 Test Equipment

The analysis equipment shall have the following attributes:

Bandwidth ≥8GHz

When clock recovery is required, the implemented clock recovery technique shall follow the JT response curve (jitter vs frequency).

Note: Clock Recovery is of 2nd Order and Loop Damping Factor is 1.43

2.2 Test Point Descriptions

Four test points have been identified for physical layer measurements. These are:

Test Point Definitions

TP1: at the pins of the transmitter device.
TP2: at the test interface on a test access fixture as close as possible to the DisplayPort mated connection to a source device
TP3: at the test interface on a test access fixture as close as possible to the DisplayPort mated connection to a sink device
TP4: at the pins of a receiving device.

These are all depicted in Figure 2-1

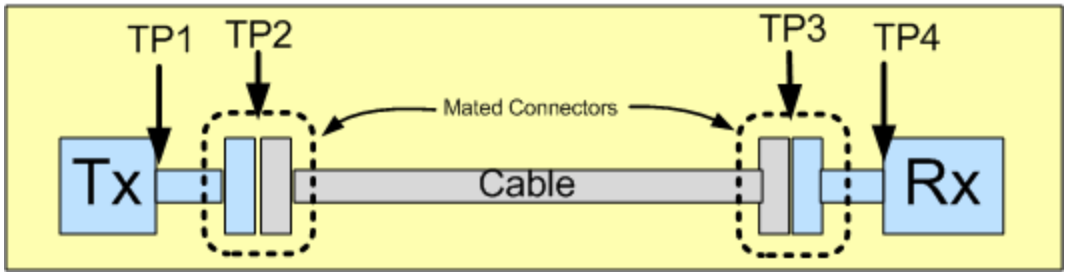

Figure 2-1: The Four Ideal Measurement Points in a DisplayPort Interconnect System

Because stimulus testing requires signal injection on the left side of TP2 and TP3 as shown in Figure 2-1 and that response testing demands connection to the right side of TP2 and TP3 as shown, for clarity, the signal injection points will be designated TP2' and TP3' while the response points will be designated TP2 and TP3. These designations are depicted in Figure 2-2 below.

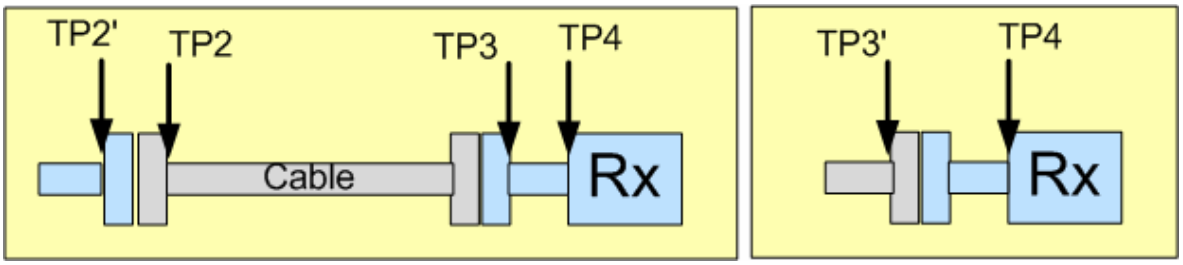

Figure 2-2: The DisplayPort Test Points

TP2 is used to access source for measurement, and TP3 is used to evaluate cable end signal or applied signal to a sink. TP2' is used for signal injection to a cable assembly or cable plus sink system. TP3' is used for signal injection to a sink device. Note that points TP2 and TP3 include whole interconnects, both plug and receptacle, and a small amount of pc board traces which can serve to degrade apparent performance slightly. Since DisplayPort physical layer testing focuses on interoperability from 'box to box' we rely exclusively on only TP2 and TP3 measurements.

Note also that we do not endeavor to establish criteria for a compliant plug or a compliant receptacle by themselves.

While we do not establish specification limits for TP1 and TP4, it is true that the tests ordained for TP2 and TP3 are useful for TP1 and TP4 as well, however, the user in such cases is obligated to understand that the limits need to be modified.

2.3 Test Point Access Fixtures

Test points TP2 and TP3 imply that a DisplayPort interconnect is made through a plug and receptacle. For the most accurate measurements, the measurement point should be as close to the interconnect junction as possible. Test point access fixtures are specialized assemblies that provide access to the signals by launching them into a connector type that is more amenable to measurement, for example SMA or SMP connectors. Test fixtures must be made as precise as possible to preserve the waveform parameters and to be as transparent as possible. Examples of how test fixtures are employed in signal analysis and injection are shown below.

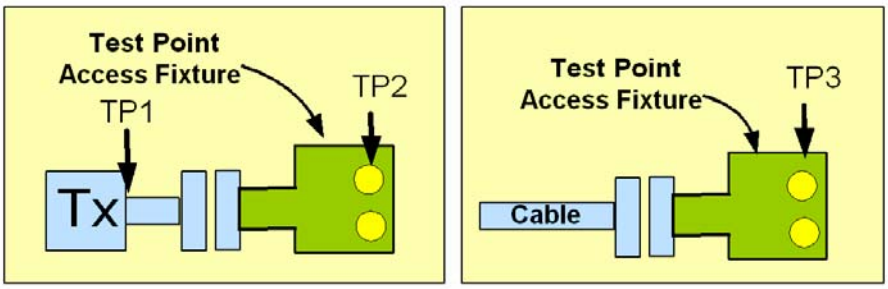

Figure 2-3: DisplayPort Test Points TP1, TP2 & TP3 with Test Point Access Fixtures

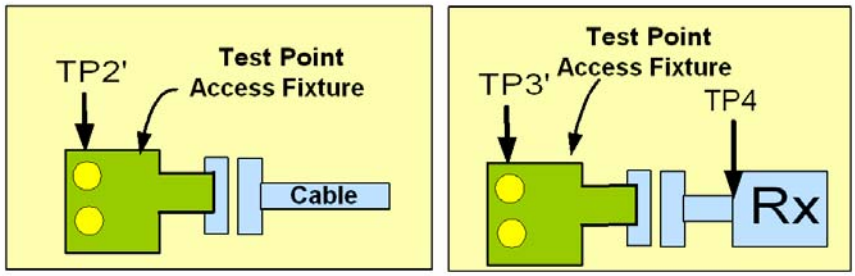

Figure 2-4: DisplayPort Test Points TP2' and TP3' for Test Signal Injection

The following is list of recommendations for the creation of such fixtures.

Recommended TPA Fixture Attributes

1. 2X thru Trace bandwidth to 6.75GHz (5th Harmonic of 2.7Gb/s)
2. Return Loss: -20dB thru 4.05 GHz (3rd Harmonic of 2.7 Gb/s) or trace impedance of 50 ohms +/- 5%
3. No deliberate mode conversion (board should employ single ended 50 ohm transmission lines over a ground plane.
4. NEXT (Crosstalk) < -40 dB thru 4.05 GHz (3rd Harmonic) into 100 ohm termination[1]
5. Calibration Structures are recommended for a PC board implementation to ascertain impedance attributes and de-embedding of transmission line effects:
   a. 1X Open trace for VNA/TDNA calibration
   b. 1X Short Trace low parasitic calibration quality for VNA/TDNA calibration
   c. 1X Load trace for 100 Ohm VNA/TDNA calibration
   d. 2X Cal trace for thru calibration, nominal impedance aberration at 50% point consistent with launch onto DisplayPort connector.

Note: Using only the structures above will not be sufficient for full de-embedding. Prior to the measurement, proper calibration shall be performed to either remove (de-embed) the effects of the test fixture through any null recognized calibration method or include the test fixture effects by implementing SOLT calibration method using standard calibration kit (supplied with the test instrument) to set up the measurement reference plane at the coaxial connectors mounted on the test fixture.

6. Skew between lanes and between individual single-ended lines of each lane shall be "Zero by design". This means that the designed trace lengths in the pc board design tool shall be precisely the same.

General

For the full suite of physical layer tests, two fixture types are required: a plug fixture and a receptacle fixture.

Preference for cal structures is to be on each fixture. Physical size realities may warrant implementation on one fixture only. The use cases requiring receptacle fixtures are size insensitive so structures are placed on these as a minimum.

Note 1: The transmission line structures above do not include a DisplayPort connector, any other connector, nor their associated copper trace footprints.

2.4 Source Control and Default Setup

The DisplayPort Source device shall be controllable over PC interface or AUX port as specified in the DisplayPort Standard. Elements controlled shall be: [Reference Table 2-48 in VESA DisplayPort Standard].

Bit Rate: 1.62 and **2.7** Gb/s

Pattern type: None, D10.2, **PRBS 7**, Symbol Error Rate pattern

Pre-Emphasis: selectable between **0**, 3.5, 6, and 9.5 dB

Differential Level: Selectable between **400**, 600, 800, or 1200mVolts peak to peak

Number of lanes: one, two or **four** lanes

Downspread Control: On/**Off**

Downspread Frequency: **30**KHz/33KHz

Bolded elements are default.

2.5 Sink Control Requirements and Default Setup

In order to verify sink performance, a source signal is applied that manifests prescribed amounts and types of jitter as well as signal level. The degraded signal, when viewed, is called a 'stressed eye'. Specifications are placed on the degradations which are listed below (Reference Table 3-13, Figure 3-21 and Tables 3-16 and 3-17 of VESA DisplayPort Standard).

Voltage Level = 150mV pk-pk +/-10% (HBR)

136mV pk-pk +/-10% (RBR)

When these degradations are manifest in an applied signal to a receiver, the receiver shall perform with a 10^{-9} (or better) bit error ratio (BER). The BER is measured by the receiving device which is queried using the control capability over the AUX port or suitable PC interface specified in the VESA DisplayPort Standard.

Table 3-13: Differential Noise Budget

	Transmitter Package Pins (INFORMATIVE)		Transmitter Connector (TP2) [NORMATIVE]		Receiver Connector (TP3) [NORMATIVE]		Receiver Package Pins (INFORMATIVE)		Notes
	Non-ISI	TJ	Non-ISI	TJ	Non-ISI	TJ	Non-ISI	TJ	
High-Bit Rate (2.7 Gbps per lane)									
A_{p-p}	0.260	0.260	0.260	0.364	0.330	0.491	0.339	0.530	1, 2, 3
Reduced-Bit Rate (1.62 Gbps per lane)									
A_{p-p}	0.160	0.160	0.160	0.223	0.442	0.539	0.465	0.580	1, 2, 3
f_{SSC}, Spread-Spectrum Modulation Frequency	30 / 33 kHz								
SSC_{tol}, Spread-Spectrum Modulation Deviation	Minimum = 5000 ppm Maximum = 0 ppm								
f_{tol}, TX Frequency Long Term Stability	Minimum = -350 ppm Maximum = 350 ppm								

Notes:

1. DisplayPort transmitter pre-emphasis must be enabled as needed in order to meet this budget specification.
2. A_{p-p} is the peak-to-peak jitter, in UI, required for the measurement points listed. The TP3 jitter properties are intended only for Sink test calibration and Hybrid-solution minimum signal consideration. This is not intended to be used as a cable qualification requirement.
3. Jitter must be measured with a second order type 2 tracking PLL configured to have a corner frequency of 20MHz (for D10.2 pattern) and damping factor of 1.428. The upper bound on this jitter measurement should be no less than the 5th harmonic of the data transmission rate.

Figure 2.5: Table 3-13 from DisplayPort Standard 1.1 Identifying Jitter Specifications

3 Source Compliance Tests

This section describes the normative and informative tests for compliance verification of DisplayPort sources. Such sources are assumed to be tested at Test Point 2 as shown below in Figure 3.1. The analyzer and the test point access fixture used are to be identified in the MOI documents from each test solution provider.

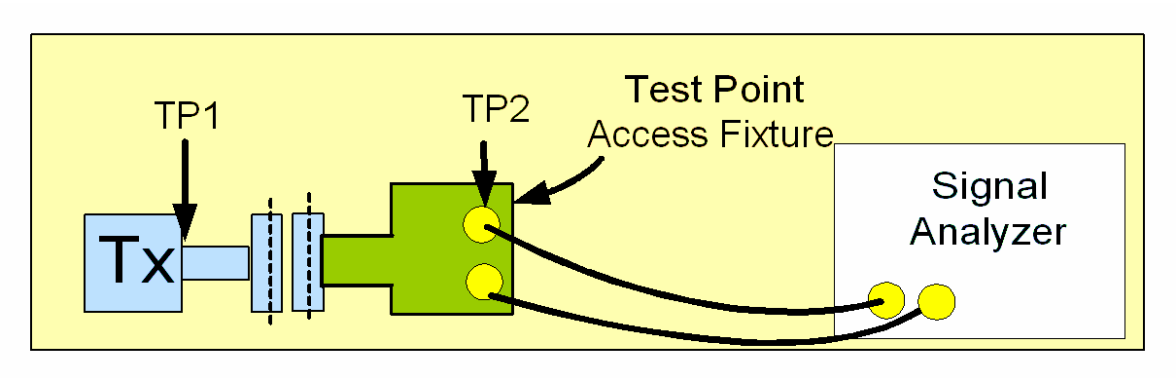

Figure 3-1: Test Point 2 Connection for Source Compliance Tests

Source Test Suite

1. Eye Diagram
2. Non Pre-Emphasis Level Verification
3. Pre-Emphasis Level Verification
4. Inter-pair Skew
5. Intra-pair Skew
6. Differential Rise Time
7. Single Ended Rise and Fall Time Mismatch
8. Overshoot and Undershoot Test
9. Frequency Accuracy
10. AC Common Mode Noise
11. Non ISI Jitter Measurement
12. Total Jitter Measurement
13. Unit Interval
14. Frequency Long Term Stability
15. Spread Spectrum Modulation Frequency
16. Spread Spectrum Deviation
17. dF/dt Spread Spectrum Deviation HF Variation

3.1 Eye Diagram Testing (Normative)

3.1.1 Test Objective

To evaluate the waveform ensuring that timing variabilities and amplitude trajectories support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

3.1.2 Interoperability Statement

The source Eye Diagram performance provides the best visual assessment of interoperability potential portraying amplitude and timing attributes of the signal and providing an intuitive understanding of design margin.

3.1.3 Test Conditions

Tests shall be conducted with 400, 600 or 800 mVolts settings for **all** Bit Rates supported **without** Pre-Emphasis.

Test Pattern = PRBS 7

3.1.4 Measurement Requirements

The following requirements must be met for each eye diagram measurement:

Clock Recovery as stipulated in section 2.1

Number of Edges measured: >100,000

Minimum Acquisition Time : 25x1/PLLBW

The Eye Diagram will be displayed such that more than one full UI is shown but no more than 2.5UI.

3.1.5 Pass/fail Criteria

For amplitude settings of 400, 600, OR 800 mVolts, the rendered eye shall have no signal trajectories entering the mask keep out area as defined by Table 3-14 for High Bit Rate and Table 3-15 for Reduced Bit Rate found in the DisplayPort Standard.

3.2 Non Pre-Emphasis Level Verification Testing (Normative)

3.2.1 Test Objective

To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven. (Reference: Table 3-10 VESA DisplayPort Standard)

3.2.2 Interoperability Statement

The source is given a range of expected output for each level setting that correlates with the system budget elements such as cable loss and receiver eye min and max values. This test ensures that the system budget is obeyed.

3.2.3 Test Conditions

Tests shall be made on **all** Bit Rates supported **without** Pre-Emphasis for all differential voltage swings supported.

Test Pattern = PRBS 7

3.2.4 Measurement Requirements

The following requirements shall be met for each level measurement:

Number of Edges measured: >1000

Amplitude measurement will be performed using $V_N = MAX(V_H,V_L)$ where V_H and V_L have the following definitions:

V_H is the Mode of the High or 'one' voltage over the last two UIs when three or more successive one's are transmitted.

V_L is the Mode of the Low or 'zero' voltage over the last two UIs when three or more successive 0's are transmitted.

Voltage Peak-Peak = V_H-V_L

3.2.5 Pass/Fail Criteria

Voltage Peak to Peak will fall in the range:

Output Level 1: 0.34≤ Result ≤0.46

Output Level 2: 0.51≤ Result ≤0.68

Output Level 3: 0.69≤ Result ≤0.92

Output Level 4: 1.02≤ Result ≤1.38

Nominal Setting is 400, 600, 800 and 1200mVolts peak-peak

3.3 Pre-Emphasis Level Verification Testing (Normative)

3.3.1 Test Objective

This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting. (Reference: Table 3-10 VESA DisplayPort Standard0.

3.3.2 Interoperability Statement

The source is given a capability to pre-emphasize the waveform to overcome deleterious effects of system losses such as through pc boards, connectors, and cables. The standard stipulates the relative magnitude to overcome specific losses. Because pre-emphasis will be negotiated, two units with substantially different degrees of pre-emphasis may be seen as non-interoperable under certain conditions. This test ensures that the system loss/pre-emphasis budget is obeyed.

3.3.3 Test Conditions

Tests shall be made on **all** Bit Rates supported **with** Pre-Emphasis for all differential voltage swings supported.

Test Pattern = PRBS7

3.3.4 Measurement Requirements

The following requirements shall be met for each level measurement:

Number of Edges measured: >1,000

Vswing measurements shall be taken using an average of a histogram of level (Vswing = Vtop - Vbase). The histogram will window the 45% to 55% locations of the analyzed bit: for transition bits, the analyzed bit is over the first bit interval past a transition; for non transition bits the analyzed bit is the third bit interval past a transition.

At every voltage setting and pre-emphasis setting subject to constraints in Table 3-12 of the DisplayPort Standard, the below measurement sequence shall be followed:

1) Set DUT with no pre-emphasis (0dB)

a. Measure the transition bit voltage swing, rail-to-rail: Vswing_transition_0dB
b. Measure the non-transition bit voltage swing (third bit of consecutive 0's or 1's): Vswing_nontransition_0dB
c. RATIO_0dB = Vswing_transition_0dB/Vswing_nontransition_0dB

2) Set DUT with pre-emphasis (PE dB=3.5, 6, or 9.5 dB)

a. Measure the transition bit voltage swing, rail-to-rail: Vswing_transition_PEdB
b. Measure the non-transition bit voltage swing (third bit of consecutive 0's or 1's): Vswing_nontransition_PEdB
c. RATIO_PEdB = Vswing_transition_PRdB/Vswing_nontransition_PEdB
d. Calculate Pre-Emphasis Ratio = RATIO_PEdB divided by RATIO_0dB.

3.3.5 Pass/Fail Criteria

1. Pre-Emphasis Calculation shall meet the following range for the appropriate levels (Reference Table 3-10 of the DisplayPort Standard).

   For 3.5 dB setting

   $1.2 \leq$ Pre-Emphasis Ratio ≤ 1.8

   For 6.0 dB setting

   $1.6 \leq$ Pre-Emphasis Ratio ≤ 2.4

   For 9.5 dB setting

   $2.4 \leq$ Pre-Emphasis Ratio ≤ 3.6

2. The values of pre-emphasis must monotonically increase as pre-emphasis setting is increased. Specifically, pre-emphasis values of 1.6 to 1.8 are valid for either the 3.5 dB setting or the 6 dB setting but NOT both.

Inter-Pair Skew Test (Normative)

3.4.1 Test Objective

To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface (Reference Table 3-10 VESA DisplayPort Standard)

3.4.2 Interoperability Statement.

The DisplayPort interface has the ability to skew, or deskew lanes by 20UI which is as much as 12ns(1.62Gb/s) and its intended operation is to eliminate simultaneous degradation of concurrent bytes of transmitted data. The specification limit of 150ps at the package pins (TP1) is likely to be degraded another 50ps passing through the connector; this is less than 0.5 UI at highest rate. It is, therefore, unlikely to be a significant reason for non-interoperability.

3.4.3 Test Conditions

Tests shall be made on **highest** Bit Rate supported **without** Pre-Emphasis for 400mvolt differential voltage swing.

Source Pattern: PRBS7

Sources with two and four lane operation only. Each combination applicable.

3.4.4 Measurement Requirements

The following requirements shall be met for the inter-skew measurement:

De-skew measurement channels

Number of Edges measured: 100

Waveform maximized on screen. More than half vertical screen used, Horizontal covers ~ 8 UI

Capture waveforms on two lanes simultaneously on two measurement channels.

Search both waveforms for common point in PRBS 7 sequence and measure time difference between the corresponding edges. Find the time of transition by determining when the waveform crosses the transition amplitude.

For each signal, find V_H and V_L using similar method as prescribed in section 3.1.4.

$V_{Transition} = \{V_H + V_L\} / 2$

Inter-Lane Skew = $\{1/NumEdges\} \sum | T_{Transition\_LaneA} - T_{Transition\_LaneB} |$

Capture waveforms on two lanes simultaneously on two measurement channels

3.4.5 Pass/Fail Criteria

$-2UI \leq$ Inter-Lane Skew – Nominal Skew setting $\leq 2UI$. The DisplayPort Standard prescribes 20UI offset from Lane 0 to Lane 1, Lane 1 to Lane 2 and from Lane 2 to Lane 3 . Between Lane 0 and Lane 2, the Nominal Skew setting will be 40UI.

3.5 Intra-Pair Skew Test (Normative)

3.5.1 Test Objective

To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface. (Reference Table 3-10 VESA DisplayPort Standard).

3.5.2 Interoperability Statement

Intra-pair skew has deleterious effects on signal rise time and manner of crossing through the transition point. The DisplayPort Standard specification at package pins (TP1) is 20 ps. It can clearly double or triple to and through the connector. These are secondary contributors to source jitter performance.

3.5.3 Test Conditions

Tests shall be made on **highest** Bit Rate supported **without** Pre-Emphasis for 400mvolt differential voltage swing.

Source Pattern: PRBS 7

Applies to one, two and four lane operation. All functional lanes to be tested.

Intra pair measurement implies two single ended probed points on a given differential data lane.

3.5.4 Measurement Requirements

The following requirements shall be met for the intra-skew measurement:

De-skew measurement channels

Number of Edges measured: Num_Edges = 100

Waveform maximized on screen. More than half vertical screen used, Horizontal covers at least on UI for good transition identification

Capture waveforms on two lanes simultaneously on two single ended measurement channels. Find falling edges that align with corresponding rising edges. Find the time of transition by determining when the waveform crosses the transition amplitude.

For each lane composed of 2 single ended signals D^+ and D^-, find V_H and V_L using similar method as prescribed in section 3.1.4.

$V_{Transition}$= 0 volts

Intra-Lane Skew = $\{1/NumEdges\}\sum | D^+_{Transition\_High} - D\text{-}_{Transition\_Low} |$

3.5.5 Pass/Fail Criteria

Intra-Lane Skew ≤ 30 ps.

.

3.6 Differential Transition Time Test (Informative)

3.6.1 Test Objective

To evaluate the lane transition (rise and fall times) of a differential data lane in a DisplayPort interface. (Reference Table 3-10 VESA DisplayPort Standard)

3.6.2 Interoperability Statement

The edge of a data signal determines how much radio frequency interference may be generated. For this reason, the edge is evaluated to be more than a minimum length.

3.6.3 Test Conditions

Tests shall be made on **all** Bit Rates supported **without** Pre-Emphasis for 400mvolt differential voltage swing.

Source Pattern: PRBS7 used in this test

Applies to one, two, and four lane operation. All functional lanes to be tested.

Differential probing across the differential lane.

3.6.4 Measurement Requirements

The following requirements shall be met for the transition time measurement:

Appropriately De-skew measurement channels

Number of Edges measured: Num_Edges = 100

Waveform maximized on screen. More than half vertical screen used, Horizontal covers at least on UI for good transition identification

Measure Vtop and Vbottom Levels: Use PRBS signal and evaluate mode of top and bottom of waveforms that exhibit at least 3 zeroes and 3 ones in a row. Use these values to set the **20/80** measurement points.

Measure transition times: Evaluate Rise and Fall times when data is 0-0-1-1 for a rise time measurement or 1-1-0-0 for a fall time measurement.

$T_{TransitionRise}$ = 1/Num rising Edges $\sum\{T_{80\%} - T_{20\%}\}$

$T_{TransitionFall}$ = 1/Num falling Edges $\sum\{T_{20\%} - T_{80\%}\}$

3.6.5 Pass/Fail Criteria

50ps $\leq$Transition Time $\leq$160ps

3.7 Single Ended Rise and Fall Time Mismatch Test (Informative)

3.7.1 Test Objective

To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface. (Reference Table 3-10 VESA DisplayPort Standard)

3.7.2 Interoperability Statement

The mismatch in time of the rising and falling time of the single-ended signals composing a differential lane will create common mode noise and will radiate.

3.7.3 Test Conditions

Tests shall be made on **all** Bit Rates supported **without** Pre-Emphasis for 400mvolt differential voltage swing.

Source Pattern: PRBS7 used in this test

Applies to one, two, and four lane operation. All functional lanes to be tested.

Two single ended signals are probed independently and acquired simultaneously and compared.

3.7.4 Measurement Requirements

The following requirements shall be met for the transition time measurement:

De-skew measurement channels

Number of Edges measured: Num_Edges = 100

Waveform maximized on screen. More than half vertical screen used, Horizontal covers at least on UI for good transition identification

Measure Vtop and Vbottom Levels: Use PRBS signal and evaluate mode of top and bottom of waveforms that exhibit at least 3 zeroes and 3 ones in a row. Use these values to set the **20/80** measurement points.

Measure transition times: Evaluate Rise and Fall times when data is 0-0-1-1 for a rise time measurement or 1-1-0-0 for a fall time measurement. For DN^+ rising and DN^- falling:

$T^+_{Transitionrising} = \{T_{20\%} - T_{80\%}\}$

$T^-_{Transitionfalling} = \{T_{80\%} - T_{20\%}\}$

$T_{DNrisingMismatch} = 1/(\text{Num } DN^+ \text{ rising Edges}) \sum (T^+_{Transitionrising} - T^-_{Transitionfalling})$

DN designates Data lane 0, 1, 2, or 3

And similarly for DN^+ falling and DN^- rising

$T_{DNfallingMismatch} = 1/(\text{Num } DN^+ \text{ falling Edges}) \sum (T^+_{Transitionfalling} - T^-_{Transitionrising})$

3.7.5 Pass/Fail Criteria

$T_{DNfallingMismatch} \leq 15\%$ of the single-ended rise time

$T_{DNrisingMismatch} \geq 15\%$ of the single-ended rise time

3.8 Overshoot and Undershoot Test (Informative)

3.8.1 Test Objective

To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.

3.8.2 Interoperability Statement

Overshoot and Undershoot are adequately discovered in an eye diagram so this test is optional.

3.8.3 Test Conditions

Tests may be made on **all** Bit Rates supported **without** Pre-Emphasis for 400mvolt differential voltage swing.

Source Pattern: D10.2 used in this test

Applies to one, two, and four lane operation. All functional lanes to be tested.

Each lane is probed differentially.

3.8.4 Measurement Requirements

The following requirements shall be met for the transition time measurement:

Appropriately De-skew measurement channels

Number of Edges measured: Num_Edges = 100

Waveform maximized on screen. More than half vertical screen used, Horizontal covers at least on UI for good transition identification

Measure Vtop and Vbottom Levels: Evaluate mode of top and bottom of waveforms to give Vtop and Vbottom. Average waveforms 100x

Measure Vmax = Maximum of waveform, Vmin = Minimum of Waveform

Overshoot% = MAX(Vmax/Vtop, Vmin/Vbottom) *100

Undershoot defined: For top half of eye: minimum value of waveform between time of maximum value and half UI point divided by Vtop.

Find time value of Vmax in waveform. Histogram vertical values between Tmax and one half UI and find minimum, Vminimum.

Undershoot%= 100*(Vtop-Vminimum)/Vtop

3.8.5 Pass/Fail Criteria

Overshoot%≤ 25 % of the differential swing

Undershoot% ≤ 25 % of the differential swing

3.9 Frequency Accuracy (Normative)

3.9.1 Test Objective

To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency. (Reference Table 3-10 VESA DisplayPort Standard).

3.9.2 Interoperability Statement

In order for sink devices to properly recover data, the source clock must operate within an acceptable tolerance to the Sink Device's recovered clock. Failure to do so can result in the inability of the Sink to properly recover the data stream.

3.9.3 Test Conditions

Tests shall be made on **all** Bit Rates supported.

Transmitter set to 0dB pre-emphasis and differential swing to maximum supported by the source.

Test Pattern = D10.2

3.9.4 Measurement Requirements

The following requirements shall be met for each frequency measurement:

Minimum Acquisition Time: 33usec

3.9.5 Pass/Fail Criteria

The mean frequency shall be within the bounds set by the bit rate +/- 300ppm not accounting for the effects of SSC.

(Reference Table 3-10 VESA DisplayPort Standard)

3.10 AC Common Mode Noise (Normative)

3.10.1 Test Objective

To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface. (Reference Table 3-10 VESA DisplayPort Standard)

3.10.2 Interoperability Statement

Mismatch between the true and complement signal of a differential pair results in common mode noise. Common mode noise can affect the sinks ability to recover valid data and may also contribute to undesirable EMI

3.10.3 Test Conditions

Tests shall be made on **all** Bit Rates supported **with** and **without** Pre-Emphasis for all differential voltage swings supported.

Test Pattern = PRBS 7

3.10.4 Measurement Requirements

The following requirements shall be met for each measurement:

Appropriately de-skew measurement channels

Number of Edges measured: >100,000

Minimum Acquisition Time : 25x1/PLLBW

$V_{TX\text{-}AC\text{-}CM} = (V_{TX\text{-}Plus} + V_{TX\text{-}Minus})/2$

3.10.5 Pass/Fail Criteria

The measured AC common mode noise shall not exceed 20mVrms.

(Reference Table 3-10 VESA DisplayPort Standard)

3.11 Non ISI Jitter Measurements (Normative)

3.11.1 Test Objective

To evaluate the amount of Non-ISI jitter accompanying the data transmission. (Reference Figure 3-18 and Figure 3-19 in the VESA DisplayPort Standard)

3.11.2 Interoperability Statement

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits violates the component level jitter budget. Non-Intersymbol Interference jitter cannot be compensated by the receiver so must be limited in magnitude.

3.11.3 Test Conditions

Tests shall be made on **all** Bit Rates supported for all output levels.

Pre-emphasis is allowed to be set for best performance. The rationale for this flexibility is the understanding that some devices may have substantial copper trace lengths to the output receptacle. In these cases, being allowed pre-emphasis to overcome the loss is reasonable.

Test Pattern = PRBS7

Signal is applied to analyzer with appropriate termination impedance.

3.11.4 Measurement Requirements

The following requirements shall be met for each frequency measurement:

Number of Edges measured: >1E6

Measurement PLL: Refer to section 2.1

Transition points in the signal (Zero crossings when signal transitions from low to high or from high to low) are found. Signal processing techniques are used to evaluate the underlying clock for the signal and the transition points are compared in time versus this time reference. Sophisticated algorithms are applied to evaluate jitter components from arrays of time deltas so determined.

3.11.5 Pass/Fail Criteria

The maximum deterministic jitter at the compliance points is outlined in the following table.

Table 3-2: Non ISI Jitter at Internal and Compliance Points.

	Transmitter package pins[1]	Transmitter Connector (TP2)	Receiver Connector (TP3)	Receiver package pins[2]
	Non-ISI	Non-ISI	Non-ISI	Non-ISI
High-Bit Rate (2.7Gb/s per lane)				
A_{TXp-p}	0.26	0.26	0.330	0.339
Reduced-Bit Rate (1.62Gb/s per lane)				
A_{TXp-p}	0.16	0.16	0.442	0.465

From Table 3-13 VESA DisplayPort Standard, consult spec for updates.

Notes: TP2 Non-ISI figures represent the normative test values for conventional source/transmitter compliance measurements. TP3 non-ISI figures represent the normative test values for Type D hybrid devices while Type T hybrid devices need to comply with TP2 specifications. All other test points are informative.

3.12 Total Jitter (TJ) Measurements (Normative)

3.12.1 Test Objective

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique[1]. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference Table 3-13 VESA DisplayPort Standard)

3.12.2 Interoperability Statement

The overall system jitter budget specifies different amounts of jitter that each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget.

Reference Jitter model in DisplayPort Standard (Section 3.5.3.8.3: The Dual Dirac Jitter Model)

3.12.3 Test Conditions

Tests shall be made on **all** Bit Rates supported.

Pre-emphasis is allowed to be set for best performance.

All voltage levels verified.

Test Pattern = PRBS 7

3.12.4 Measurement Requirements

The following requirements shall be met for each Total Jitter measurement:

Number of Edges measured: >1E6

Measurement PLL : Refer to section 2.1)

Use Dual Dirac Model to estimate jitter to a 10^{-9} BER.

Transition points in the signal (Zero crossings when signal transitions from low to high or from high to low) are found. Signal processing techniques are used to evaluate the underlying clock for the signal and the transition points are compared in time versus this time reference. Sophisticated algorithms are applied to evaluate jitter components from arrays of time deltas so determined.

3.12.5 Pass/Fail Criteria

The maximum total jitter at the compliance points is outlined in the following table.

[1] Approved TJ estimation methods are outlined in Fibre-Channel Methodologies for Jitter and Signal Quality Specification- MJSQ Revision 14.1 June 5 2005.

Table 3-3: Total Jitter at Internal and Compliance Points

	Transmitter package pins[1]	Transmitter Connector (TP2)	Receiver Connector (TP3)	Receiver package pins[2]
	TJ	TJ	TJ	TJ
High-Bit Rate (2.7Gb/s per lane)				
A_{TXp-p}	0.26	0.364	0.491	0.53
Reduced-Bit Rate (1.62Gb/s per lane)				
A_{TXp-p}	0.16	0.223	0.539	0.58

From Table 3.13 VESA DisplayPort Standard

Notes: TP2 TJ figures represent the normative test values for conventional source/transmitter compliance measurements. TP3 TJ figures represent the normative test values for Type D hybrid devices while Type T hybrid devices need to comply with TP2 specifications. All other test points are informative.

3.13 Unit Interval (Normative)

3.13.1 Test Objective

To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM

3.13.2 Interoperability Statement

This test ensures that with Spread Spectrum Clocking there is not excessive unit interval error due to high frequency content that may not be trackable.

3.13.3 Test Conditions

Tests shall be performed on a PRBS7 signal, with SSC enabled. An evaluation of at least 100K Unit Intervals or 1 Full SSC cycle is required to ensure that any SSC modulation on the signal does not violate the timebase accuracy specifications.

3.13.4 Measurement Requirements

This measurement should be evaluated over 100K Consecutive Unit intervals. The execution of this test must include use of a high pass filter to remove the low frequency SSC components of phase modulation. This filter is a High Pass filter with a 20dB/Decade roll-off with a corner frequency 60X that of the highest SSC frequency allowed (1.98MHz).

3.13.5 Pass/Fail Criteria

The mean Unit Interval must satisfy the following criteria.

- Mean Unit Interval measured between 617.0678ps (min) to 620.5863ps (max) (for products running at RBR).

- Mean Unit Interval measured between 370.2407ps (min) to 372.3518ps (max) (for products running at HBR)

3.14 Frequency Long Term Stability (Normative)

3.14.1 Test Objective

To evaluate the overall variation in source timebase accuracy over a measurement interval of no fewer than 10 SSC cycles, ensuring the device stays within the required +- 300PPM limit.

3.14.2 Interoperability Statement

Excessive variation in the bit rate will reduce capability of receiver tracking

3.14.3 Test Conditions

Tests shall be performed on a PRBS7 signal, with SSC enabled. An evaluation of at least 10 full SSC cycles is required.

3.14.4 Measurement Requirements

As SSC in Display Port is mandatory, the reported result must be the mean of ten measured maximum values from the range of SSC modulation deviation. The execution of this test must include use of the filter to remove the low frequency SSC components of phase modulation. This filter is a High Pass filter with a 20dB/Decade roll-off with a corner frequency 60X that of the highest SSC frequency allowed. (1.98MHz).

3.14.5 Pass/Fail Criteria

Pass/Fail Criteria
f_{tol} measured between -300ppm and 300ppm.

3.15 Spread Spectrum Modulation Frequency (Normative)

3.15.1 Test Objective

To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.

3.15.2 Interoperability Statement

SSC frequency has relatively little effect on interoperability.

3.15.3 Test Conditions

The SSC frequency will be evaluated at the highest bitrate the transmitter supports. Tests shall be performed on a PRBS7 signal, with SSC enabled. An evaluation of at least 10 full SSC cycles is required (Mean value reported).

3.15.4 Measurement Requirements

As SSC in DisplayPort is mandatory, the reported result must be the mean of ten measured maximum values from the range of SSC modulation deviation.

3.15.5 Pass/Fail Criteria

f_{SSC} measured between 30kHz and 33kHz
The value above shall be based on a mean of at least 10 complete SSC cycles

3.16 Spread Spectrum Modulation Deviation (Normative)

3.16.1 Test Objective

To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.

3.16.2 Interoperability Statement

Spread Spectrum clocking spectrum is a system performance issue. Interoperability risk is low.

3.16.3 Test Conditions

The SSC Modulation Deviation will be evaluated at the highest bit rate the transmitter supports.

Tests shall be performed on a PRBS7 signal, with SSC enabled.

An evaluation of at least 10 full SSC cycles is required (Mean value reported).

3.16.4 Measurement Requirements

As SSC in DisplayPort is mandatory, the reported result must be the mean of ten measured maximum values from the range of SSC modulation deviation.

The value reported as the result must be the single total range value relative to nominal of the SSC modulation deviation, using the equation below, where "Min" is the mean of 10 recorded values of the minimum peaks.

Calculate deviation = (Measured Min – Nominal)/Nominal * 1e6 ppm

3.16.5 Pass/Fail Criteria

SSC_{tol} measured (using mean of 10 recorded values) between -5000ppm and +0ppm.

3.17 dF/dt Spread Spectrum Deviation HF Variation (Informative)

3.17.1 Test Objective

Verify SSC profile does not include any frequency excursions which would exceed 1250ppm/uSec.

3.17.2 Interoperability Statement

Product interoperability will be greatly reduced possibly to the point of failure if the SSC profile modulated on to the transmitter data signals does not follow a conventional triangular of Lexmark profile. Rapid variations or low frequency phase noise will results in frequency variation spurs will be exposed by this test and product which exceed the specified 1250ppm/uSec rate of variation will be considered non-compliant.

3.17.3 Test Conditions

The SSC dFdT limit will be evaluated at the highest bitrate the transmitter supports.

Tests shall be performed on a PRBS7 or a Clock signal, with SSC enabled.

An evaluation of at least 10 full SSC cycles is required (peak dFdT value reported).

3.17.4 Measurement Requirements

The execution of this test must include use of the low pass filter to remove the high frequency non SSC jitter components. This low pass filter will be a 2^{nd} order Butterworth with a 3dB corner frequency set at 60X that of the highest SSC frequency allowed. (1.98MHz). This analysis will be conducted over a minimum of 10 full SSC cycles.

The difference between any two frequency values separated by 1uSec, shall be no greater than 1250 ppm.

3.17.5 Pass/Fail Criteria

SSC_t DfDt must not exceed 1250pmm/usec variation.

4 Sink Compliance Tests

This section describes the normative and informative tests for compliance verification of DisplayPort receivers. Such receivers are assumed to be tested at Test Point 3 as shown below in Figure 4-1.

Shown in this figure is an AUX Channel connection which is used to control the Receiver DUT and to query DPCD registers for bit error count. The calibrated stimulus instrument and test point access fixture used are identified in the MOI documents from each test provider.

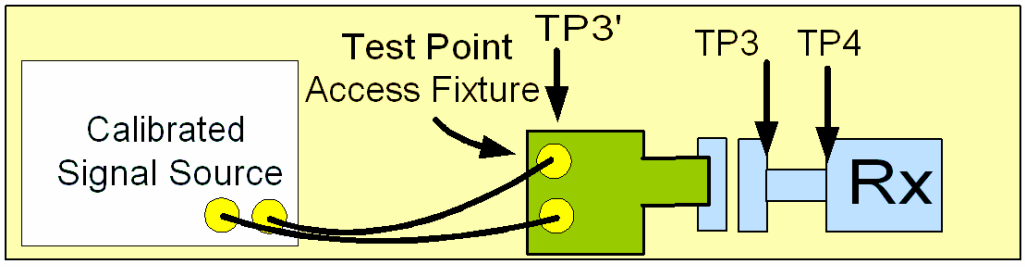

Figure 4-1: Test Point 3' (TP3') Connection for the Receiver Compliance Tests

Sink Test Suite

1. Sink Jitter Tolerance Testing

4.1 Sink Jitter Tolerance Test (Normative)

4.1.1 Test Objective

The DisplayPort Standard outlines a minimum Receiver Eye diagram (DisplayPort Standard Figure 3-21) which is measured at the receiver silicon component junction. This test is designed to provide an impaired stimulus which has been calibrated to the minimum TP3 connector electrical properties.

These properties are defined in Table 3.11 and Table 3.13 and differ for High Bit Rate (HBR, 2.7GB/s) and Reduced Bit Rate (RBR, 1.62GB/s) transmission speeds. This test outlines the pass fail criteria around these tests. (Reference Section 3.5.3 of DisplayPort Standard)

4.1.2 Interoperability Statement

This test will test the receiver ability to sustain a 10E-9 BER under the most egregious signaling conditions permitted by the specification.

The receiver tolerance to the applied test vector varies as a function of the test signals fundamental jitter component as explained in Section 3.5.3.8.1 of the DisplayPort Standard.

The following jitter tolerance mask JTHBRrx applies for a PRBS7 test vector at High Bit Rate:

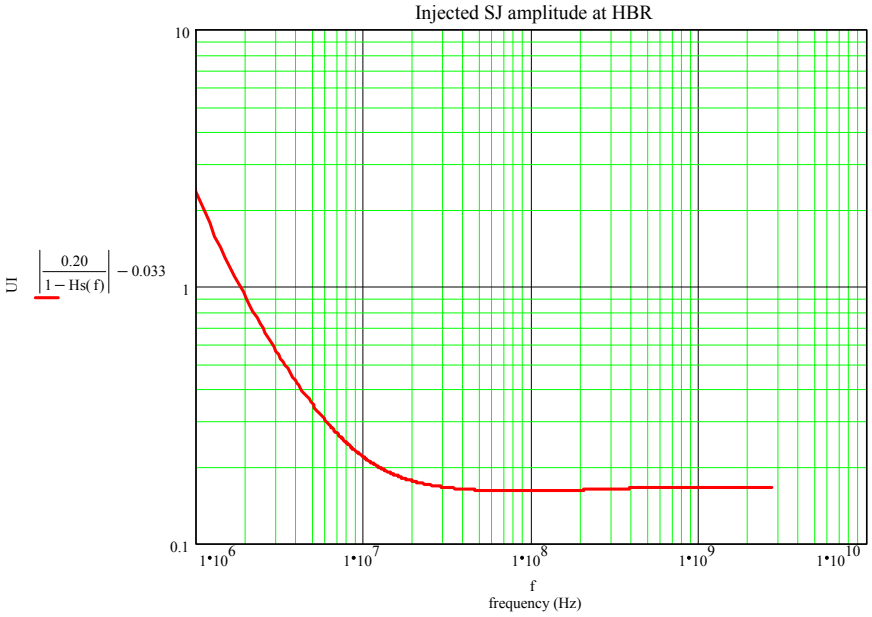

Figure 4-2: JTHBRx Curve from DisplayPort Standard. Sinusoidal Jitter Tolerance Curve vs Frequency for High Bit Rate.

The following jitter tolerance mask JTRBRrx applies for a PRBS7 test vector at Reduced Bit Rate:

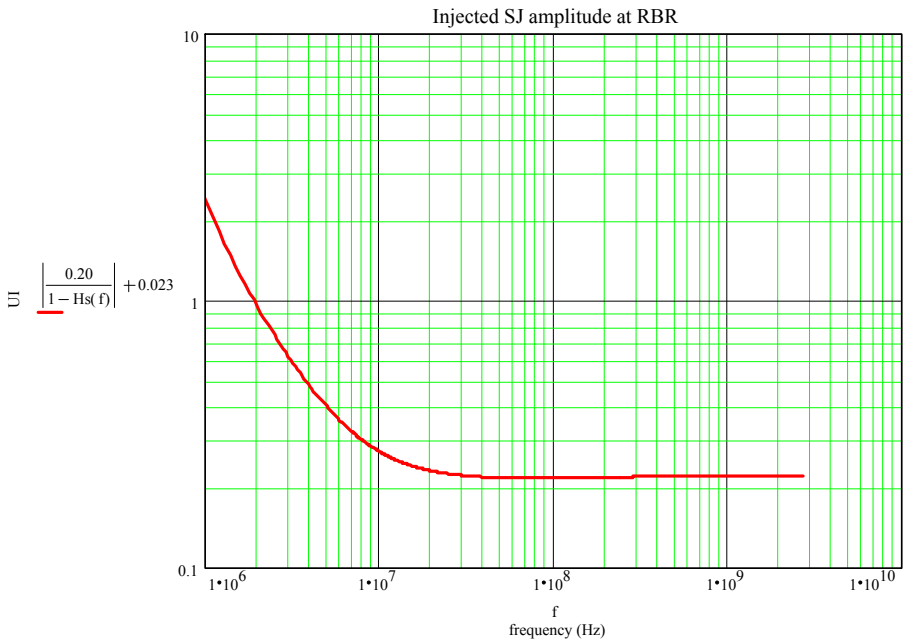

Figure 4-3: JTRBRx Curve from DisplayPort Standard. Sinusoidal Jitter Tolerance vs Frequency for Reduced Bit Rate

The magnitude of Tj and Dj must be managed to sustain a level below the JTHBRrx and JTRBRrx tolerance curves.

4.1.3 Test Conditions

The test shall be performed for all lanes of a receiver. Each lane is tested individually while adjacent lanes will have a clock pattern injected to simulate cross-talk effects on the receiver's PCB.

Note: The DisplayPort Standard requires sink devices to support link training and PRBS7 test on individual lanes.

The amplitude of the applied signals shall be: (specified in section 2.5)

High Bit Rate: voltage = 150mVolts peak-peak (Table 3-16 of DisplayPort Standard)

Reduced Bit Rate: voltage = 136mVolts peak-peak. (Table 3-17 of DisplayPort Standard)

The peak to peak voltage shall be measured by as the difference between V_{pulse}+ and V_{pulse}- where each is evaluated as the the mode of the voltage of an isolated pulse at the end of 4-1-1 run length sequence. Vpulse+(0,0,0,0,1,0) and Vpulse-(1,1,1,1,0,1).

No pre-emphasis or spread spectrum clocking shall be present on the applied signal. Tests are conducted at each jitter frequency specified.

Note: Other standards are being followed with respect to Spread Spectrum Clocking. This requirement may change in the future.

The following table identifies the test parameters:

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR RBR	2 MHz	10^{12}	1000	HBR=370 RBR=620	0
HBR RBR	10 MHz	10^{11}	100	HBR=37 RBR=62	+350ppm +350ppm
HBR RBR	20 MHz	10^{11}	100	HBR=37 RBR=62	0
HBR	100 MHz	10^{11}	100	HBR=37	0
1. To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds					

The receiver tolerance test will be formed on a statistically relevant population of data. Two populations will be used. One is 1000 times the 1/Bit Error Rate (Bit Error Rate = 10^{-9}) during which fewer than 1000 receiver errors shall be observed. 10^{12} bits requires a direct test time of 370 seconds at HBR rates and 620 seconds at RBR rates.

A second population is 100 times the 1/Bit Error Rate during which fewer than 100 receiver errors shall be observed. 10^{11} bits requires a direct test time of 37 seconds at HBR rates and 62 seconds at RBR rates.

The rationale for having two populations is to test in an appropriate amount of time:

1. With long observations times over which infrequent system behaviors may become manifest, and,
2. To test several frequencies to evaluate the PLL frequency response.

The stress pattern used shall be the PRBS7 as defined in Table 2-48 of the DisplayPort Standard.

Note: Receivers implement a PRBS7 bit error counter. Thus the PRBS7 test results can be related directly to a meaningful bit error ratio (BER) by keeping track of the observation time. That BER directly compares against the target BER and serves as a pass/fail criteria.

Jitter will be injected in accordance with the given jitter tolerance masks JTHBRrx and JTRBRrx. The stressed signal shall be calibrated at TP3 to a total jitter Tj of 10% below the jitter tolerance mask.

The stressed signal generator (SSG) shall be calibrated before this test is performed. As the reference plane TP3 for sink device test cannot be directly measured, a DisplayPort to SMA fixture will be needed to calibrate the stressed signal.

As part of the calibration procedure, jitter is measured with a clock to data method. Therefore the SSG outputs a clean (i.e. having random jitter less than one-fourth of ultimately applied random jitter) clock signal that will be used by a jitter measurement device (JMD) to determine the injected jitter.

The following figure outlines the calibration setup. The same setup also serves to calibrate the minimum eye opening. All calibrations are performed using a PRBS7 pattern.

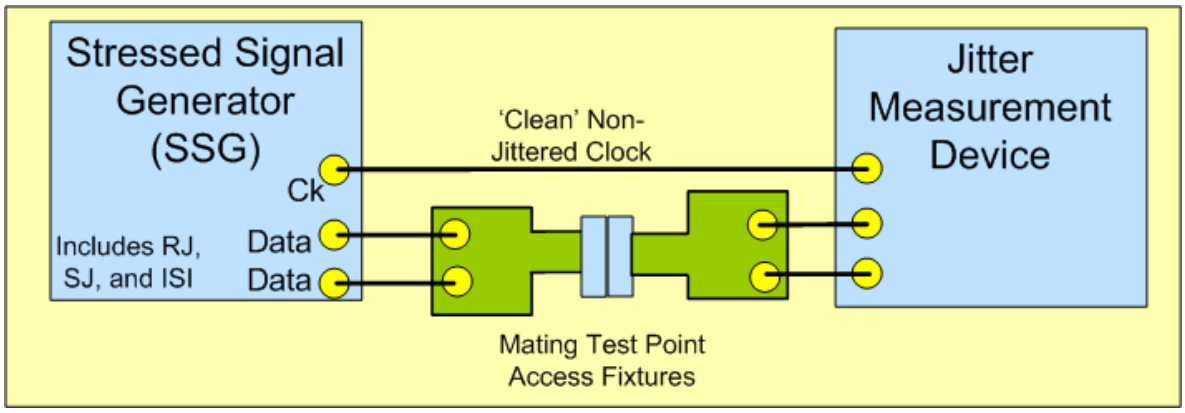

Figure 4-4: Jitter Tolerance Testing Calibration Setup

The injected jitter is composed of three elements: Inter-symbol Interference (ISI), Random Jitter (Rj), and Sinusoidal Jitter (Sj). While the ISI and Rj elements are kept constant Sj will differ based on its modulation frequency to achieve the required Tj. Assuming a jitter model of: 12.3Rj(RMS) + Dj = Tj, the following settings have to be tested for reduced bit rate:

f(Sj)	Tj(JTRBRrx)-10%	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1268.9	97	17.8	953
10	589.9	97	17.8	274
20	546.9	97	17.8	231

Table 4-2: Jitter Component Settings for Reduced Rate

The following settings also must be tested for high bit rate:

Table 4-3: Jitter Component Settings for High Rate

f(Sj)	Tj(JTHBRrx)-10%	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1220.4	161	13.2	897
10	541.4	161	13.2	218
20	498.4	161	13.2	175
100	484.4	161	13.2	161

In order to achieve a Tj-10% ISI and RJ shall be calibrated to the given value and then SJ shall be increased until a Tj-10% is achieved. Thus the actual SJ will be lower than shown in Table 4.2 and Table 4.3

For sink device test, it is essential to cover crosstalk effects on the receiver board. A half-rate clock signal (D24.3 pattern) is injected to lanes that are adjacent to the lane under test. For High Bit Rate this signal has a frequency of 1.35GHz(Bit rate divided by 2) while for Reduced Bit Rate the signal has a frequency of 810MHz.

It is an important requirement that crosstalk must not be phase aligned with the stressed signal, and that its phase is sufficiently random over the observation period. As the stressed signal is 'jittered' the crosstalk clock signal may be a 'clean' (i.e. low jitter) signal.

Note: Having the 'clean' signal slightly off frequency(i.e.3-5%) will achieve the recommended random phase characteristics..

Note: the crosstalk requirement does not apply to receivers that have only one lane. For sink devices with two lanes the lane that is not under test will receive the D24.3 pattern. Sink devices with four lanes will be tested four times using the following scheme:

- Lane 0 under stressed signal: D24.3 to lane 1 and 3, no signal to lane 2
- Lane 1 under stressed signal: D24.3 to lane 0 and 2, no signal to lane 3
- Lane 2 under stressed signal: D24.3 to lane 1 and 3, no signal to lane 0
- Lane 3 under stressed signal: D24.3 to lane 0 and 2, no signal to lane 1

4.1.4 Measurement Requirements

Receiver stress test is separated in multiple phases. First the signal generator initiates link training for the lane under test. Once link training is performed the pattern is changed to PRBS7 and it is verified that the sink device's PRBS7 counter actually works properly. Link training and counter operation are pass/fail criteria. After these verifications receiver stress tests with signals with specified level and jitter are performed. During these tests the number of bit errors are counted over a specified time interval. The total number of errors is compared against the specified value.

Note: It is a requirement for the SSG to change pattern and turn on/off Rj and Sj without any interruption. This means that when transitioning between pattern that there be no disruption in clock frequency or symbol clocking integrity and when transitioning between jitter states that there be no disruption in data pattern or clock frequency.

Link training is done in two phases: the frequency lock phase and the symbol lock phase. Both phases require the SSG to send the necessary pattern as defined in the DisplayPort Standard specification. Link training is performed with ISI, Rj and SJ injected. SJ has to be at the highest frequency for the tested data rate. This is required for the sink device to choose the appropriate equalization settings. The SSG has to be able to change between the required modulation frequencies for SJ seamlessly as SJ will be at the highest frequency during link training and may be reduced to a lower frequency for the BER test. It is anticipated for all tests to use the AUX channel to control the sink device and to read the PRBS7 counter. If no such tool is available, a vendor- specific debug tool may be used.

The following figure outlines the test setup in principle. It illustrates an example where the sink device has 4 lanes and lane 1 is under test.

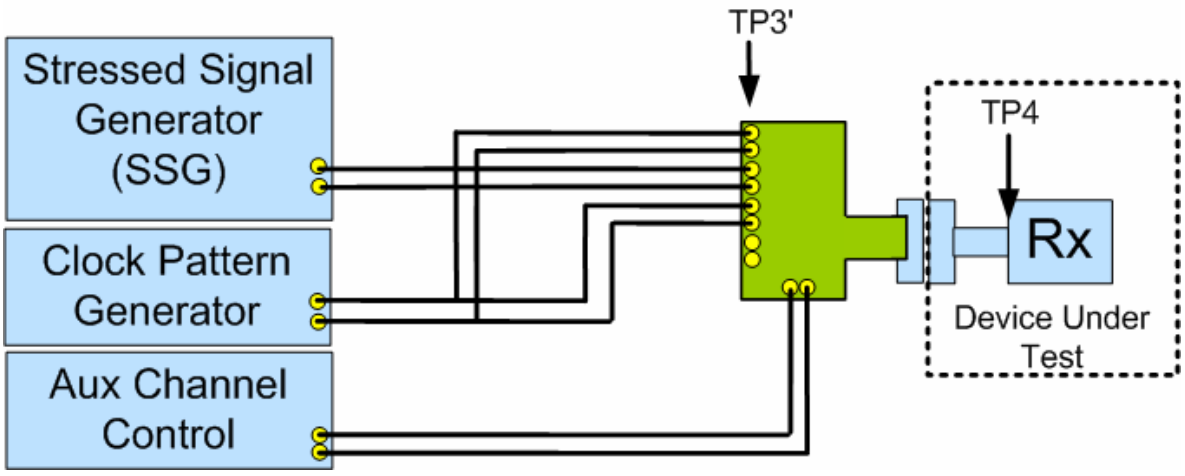

Figure 4-5: Jitter Test Setup

The following procedure applies for each lane:

1. Connect the SSG to the lane under test and clock pattern generator to the adjacent lanes. Adjust data rates for Reduced Bit Rate or High Bit Rate. All jitter sources and minimum eye were calibrated previously. ISI and Rj are turned on. SJ is turned on at the highest frequency (i.e 100MHz for HBR and 20 MHz for RBR).

   Frequency lock phase

2. SSG outputs a D10.2 clock pattern (includes injected ISI, Rj and Sj jitter).
3. AUX Control initiates the frequency lock phase
4. After >100us AUX Control verifies whether DUT achieved frequency lock. If not go to the previous step. If frequency lock cannot be achieved within 5 retries (with maximum consecutive AUX Defers allowable = 8) the test result shall be a failure. Lock is verified by polling CR_LOCK status for the data

lane under test:
If LANE0_CR_DONE (Address202h bit 0) = 1
If LANE1_CR_DONE (Address202h bit 4) = 1
If LANE2_CR_DONE (Address203h bit 0) = 1
If LANE3_CR_DONE (Address203h bit 4) = 1

Symbol lock phase

5. SSG outputs symbol lock pattern as defined in specification with ISI, Rj and SJ jitter injected
6. AUX Control initiates the symbol lock phase
7. After >100us AUX Control verifies whether DUT achieved symbol lock. If not go to the previous step. If symbol lock cannot be achieved within 5 retries (with maximum consecutive AUX Defers allowable = 8) the test result will be a failure. Lock is verified by polling CR_LOCK status for the data lane under test:
   If LANE0_CHANNEL_EQ_DONE (Address202h bit 1)
   If LANE0_SYMBOL_LOCKED (Address202h bit 2)
   If LANE1_CHANNEL_EQ_DONE (Address202h bit 5)
   If LANE1_SYMBOL_LOCKED (Address202h bit 6)
   If LANE2_CHANNEL_EQ_DONE (Address203h bit 1)
   If LANE2_SYMBOL_LOCKED (Address203h bit 2)
   If LANE3_CHANNEL_EQ_DONE (Address203h bit 5)
   If LANE3_SYMBOL_LOCKED (Address203h bit 6)

PRBS7 counter test phase

8. SSG outputs PRBS7 pattern as defined in specification with ISI, Rj and SJ jitter injected
9. AUX Control initiates and clears the PRBS7 error counter
10. SSG injects one single bit error while looping the PRBS7 pattern (I.e. in subsequent repetitions of the PRBS7 pattern only once the PRBS7 pattern shows one wrong bit)
11. AUX Control verifies that the PRBS7 counter shows one bit error. If not the test result will be a failure.

BER test phase

12. Stressed Signal Generator outputs PRBS7 pattern as defined in specification with Rj, Sj, and ISI jitter injected. The SJ frequency has to be set to the current test case.
13. AUX Control clears the PRBS7 error counter
14. Run test for specified time

The PRBS7 error counter is read through AUX Channel Control.

4.1.5 Pass/Fail Criteria

For each lane and all supported data rates:

- The receiver is required to achieve frequency lock and symbol lock within 5 retries.
- The PRBS7 counter has to be operational.
- Number of Errors as depicted in Table 4-4

Table 4-4: Maximum Allowable Errors for Each Data Rate and Jitter Frequency

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable
HBR RBR	2 MHz	10^{12}	1000
HBR RBR	10 MHz	10^{11}	100
HBR RBR	20 MHz	10^{11}	100
HBR	100 MHz	10^{11}	100

5 Cable Compliance Tests

This section defines the electrical components and specification of the passive cable adaptor and the cable adaptor discovery mechanism. As it is likely that a cable manufacturer will have a number of lengths of a given cable construction to be certified compliant, each length would normally be required to undergo the full cable test regimen.

In the interest of complete testing of cables for compliance, we mandate that all cable assemblies of a vendor's cable construction family shall be tested. (In the future, when full understanding of cable performance is known, only representative units of a cable family may be chosen for compliance test). It is then necessary to define cable assembly and cable construction family:

Cable Assembly

The cable assembly includes the following.

1. Bulk Cable
2. Two fully mated DisplayPort connectors [both ends of cable]
3. Any intervening cable management constructs such as paddle card assemblies (Note, paddle cards are part of the connector, not the bulk cable from a measurement standpoint.

The cable assembly begins and ends at the edges of the PCB board where the DisplayPort receptacle plug solder pads reside. The solder pads are considered part of the connector.

Cable Family

A cable family includes the following:

1. Common cable physical construction--- this includes the same wire gauge, same dielectric/insulators, equalization implementation, and the same cross sectional attributes.
2. Common manufacturing processes: this includes but not limited to cable management, soldering process, cable alignment or other control parameters.
3. No variation in equalization (if used) is allowed

Note: It is expected that cables that are tested for compliance reflect the normal production processes that will be used for that family of cables.

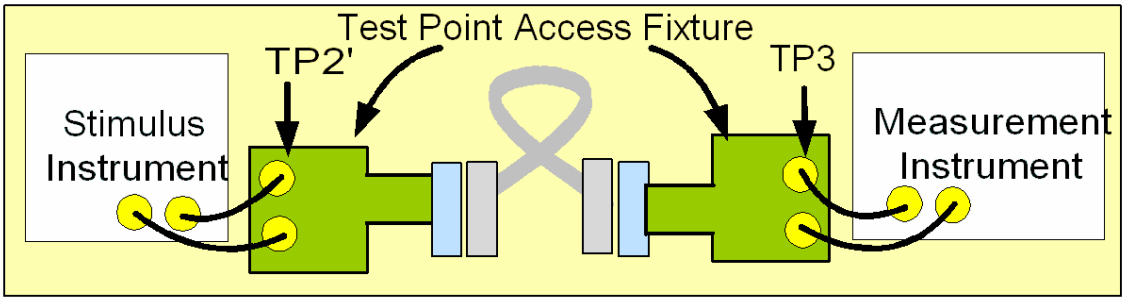

Figure 5-1: Cable Test Configuration with Two Test Point Access Fixtures

The test target for these compliance tests are complete cable assemblies. No effort will be made to perform interoperability or compliance on individual components.

Cable Test Suite

1. Cable Assembly Inter-pair Skew
2. Cable Assembly Intra-Pair Skew
3. Far End Noise (FEN)
4. Bulk Cable and Connector Impedance
5. Insertion Loss (IL/SDD21)
6. Near End Noise (NEN)
7. Return Loss (RL/SDD11)

5.1 Cable Assembly Inter-pair Skew Measurements (Informative)

5.1.1 Test Objective

The inter-pair skew measurement (time skew between two differential lanes) must not exceed 2 UI.

(Reference Figure 4-9 in Section 4.1.5.4.2 (Inter-Pair Skew for Cable Assembly) in the VESA DisplayPort Standard).

5.1.2 Interoperability Statement

Inter-pair skew defines the difference between the minimum and maximum delay times for transmitted signals along the group of channels which make up the system. The inter-pair skew has its origin in electrical length differences, typically due to physical length differences between channels, or differences in the impedance encountered by the signal transmitted through different channels.

The purpose of the specification limit is to ensure that the signals arrive at the receiver within the designated timing window to avoid timing and logic errors within the system.

5.1.3 Test Conditions

If a family of cables is being tested, only the longest length is tested for this requirement.

Cable will be un-rolled and made relatively straight (minimum bend radius of .5m) before making these measurements. Adjacent unused channels shall be terminated into suitable 50 ohm loads.

5.1.4 Measurement Requirements

Special attention to the fixtures is required in performing skew measurements. The instrument grade receptacle fixture with no cable present should be de-skewed appropriately before performing this measurement.

This measurement should be conducted from the non-equalized end of a cable should one exist.

5.1.5 Pass/Fail Criteria

The observed intra-pair skew should be measured and be less than 2 UI using the method outlined in Figure 5-2.

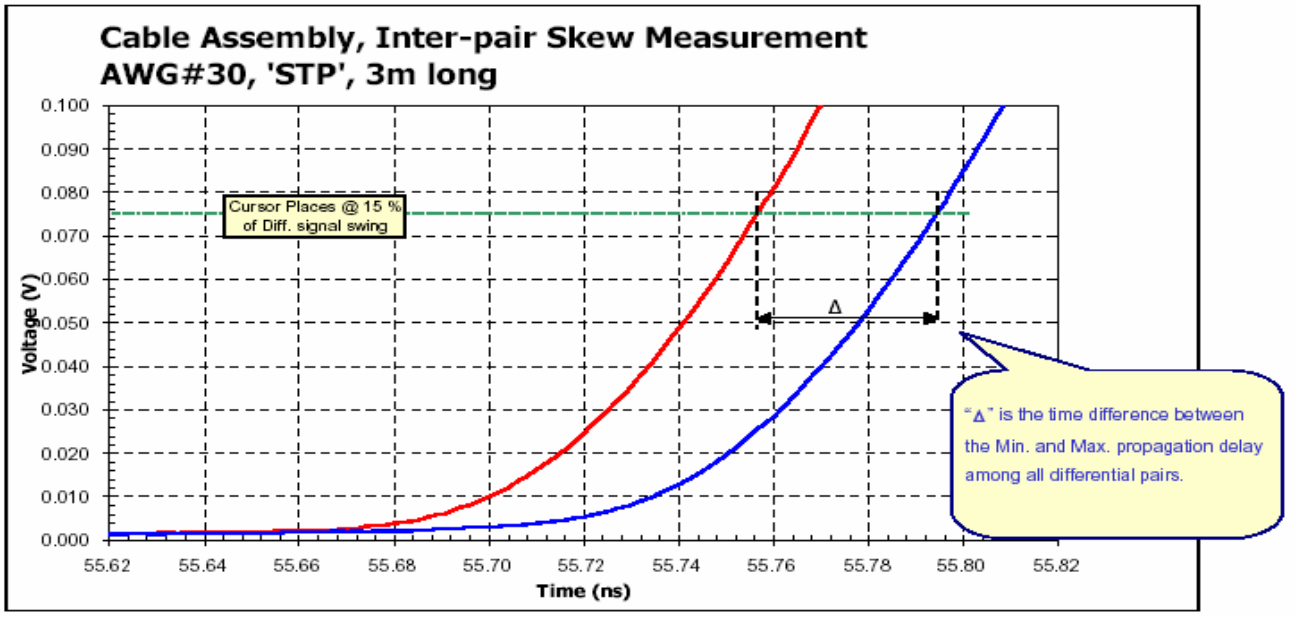

Figure 5-2: Inter-Pair Skew Measurement Method.

Reference DisplayPort Standard 4.1.5.4.2.

5.2 Cable Assembly Intra-pair Skew Measurements (Normative)

5.2.1 Test Objective

The intra-pair skew measurement (skew between common D+ and D- conductors in the cable) can not exceed 50ps.

(Reference Figure 4-8 in section 4.1.5.4.1 (Intra-Pair Skew for Cable Assembly) in the VESA DisplayPort Standard)

5.2.2 Interoperability Statement

Intra-pair skew defines the difference between the minimum and maximum delay times for transmitted signals along lines within a channel. Excessive intra-pair skew can severely distort the rising edge of the signal, causing increased rise time degradation, increased ISI, and increased jitter, leading to an un-recoverable signal at the receiver. Further, excessive intra-pair skew can lead to significant differential to common mode conversion, causing increased differential channel loss and potential EMI issues due to common mode noise.

The purpose of the specification limit is to ensure that electrical mechanical characteristics of the channel are controlled to that extent that it provides a homogeneous transmission environment for both lines of the channel such that the signal may be accurately recovered at the receiver.

5.2.3 Test Conditions

If a family of cables is being tested, only the longest length is tested for this requirement.

Cable will be un-rolled and made relatively straight (minimum bend radius of .5m) before making these measurements. Adjacent unused channels shall be terminated into suitable 50 ohm loads.

5.2.4 Measurement Requirements

Special attention to the fixtures is required in performing skew measurements. The instrument grade receptacle fixture with no cable present shall be de-skewed appropriately before performing this measurement.

This measurement should be conducted from the non-equalized end of a cable should one exist.

5.2.5 Pass/Fail Criteria

The observed Intra-pair skew shall be less than 50ps using the method outlined in Figure 5-3.

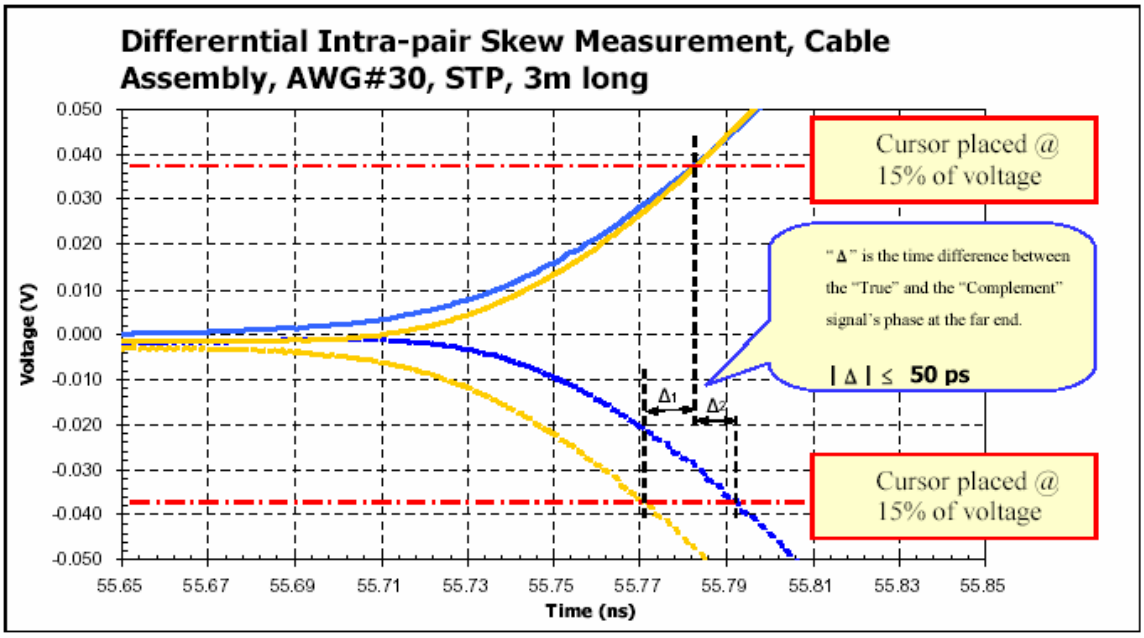

Figure 5-3: Intra-Pair Skew Measurement Method.

Reference DisplayPort Standard 4.1.5.4.1

5.3 Far End Noise (FEN) Measurements (Normative)

5.3.1 Test Objective

The DisplayPort Standard outlines two *identical* Far End Noise (FEN) profiles. One of the high bit rate cable assembly and one corresponding profile for the lower bit rate cable assembly. This test outlines the pass fail criteria around these two tests.

(Reference Figures 4-7 and 4-13 (Far End Total Noise (peak) HBR/RBR Cable Assembly FEN profiles) in the VESA DisplayPort Standard).

5.3.2 Interoperability Statement

Far end differential noise defines the magnitude of the inductive and capacitive coupled noise from a driven "aggressor" channel (or channels) on to a quiet "victim" channel. Far end noise specifically refers to the differential noise level measured on the victim channel at the sink side of the channel, relative to a differential signal or signals originating at the source side of an aggressor channel (or channels). For multiple aggressors the resultant far end noise is the magnitude sum of the individual differential noise components of the aggressor channels. Far end noise can significantly distort the received signal leading to jitter and ISI issues for the received signal on the victim channel.

The purpose of the specification limit is to ensure that the level of differential noise seen by a signal on the "victim" channel due to far end noise coupling is below a maximum allowable level necessary to ensure that an accurate representation of the input signal can be recovered by the receiver.

5.3.3 Test Conditions

If a family of cables is being tested, only the longest length is tested for this requirement.

FEN is a cross channel SDD21 (near end to far end) measurement and shall be evaluated and compared to the corresponding limits mask, from 100MHz to 7 GHz)

Cable will be un-rolled and made relatively straight (minimum bend radius of 0.5m) before making these measurements.

This is either a single or dual adjacent aggressor (either side) test as illustrated in Figure 5-4 and Figure 5-5. AUX channel is included in this FEN. Two worst case aggressors' magnitudes (linear) can be added together if measured separately.

Asynchronous noise is the aggressor.

Channel pairs to test against either one or two worst case aggressors based on the following combinations

Test #	Aggressor(s) Channel(s)	Victim Channel
1	Main Link(1)	Main Link(0)
2	Main Link(0) + Main Link(2)	Main Link(1)
3	Main Link(1) + Main Link(3)	Main Link(2)
4	Main Link(2) + AUX Ch.	Main Link(3)
5	Main Link(3)	AUX Ch.

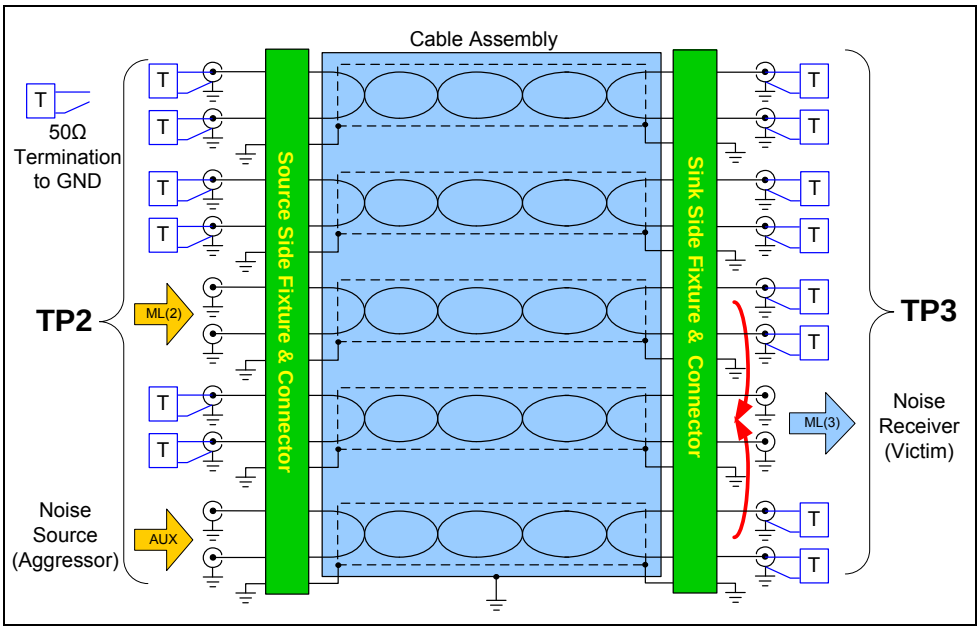

Figure 5.4: Far End Total Noise (peak) Typical Dual Aggressor configuration

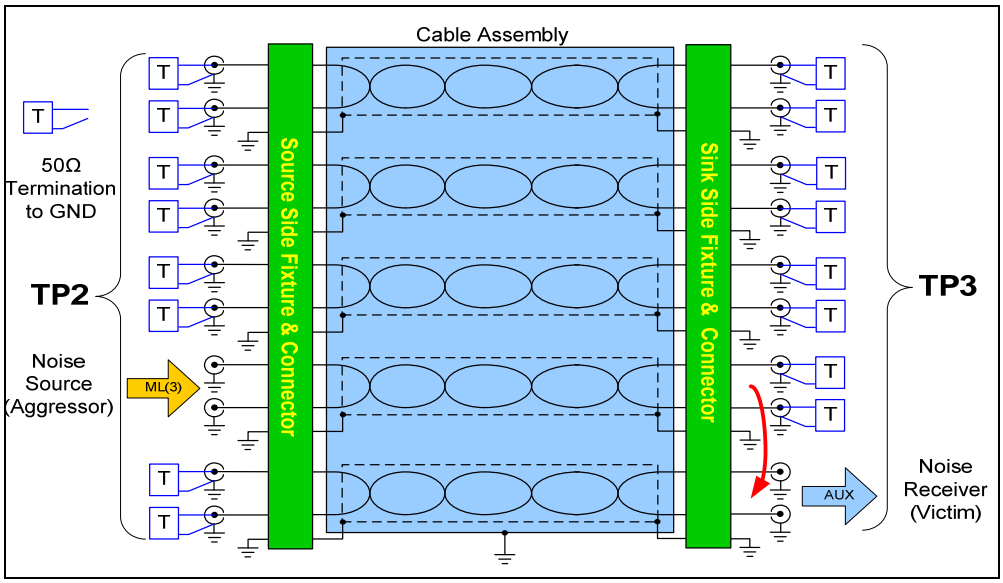

Figure 5.5**: Far End Total Noise (peak) Typical Single Aggressor configuration**

5.3.4 Measurement Requirements

Special attention to the fixtures is required in performing FEN measurements. The figure of merit to determine if a fixture is suitable to perform a FEN measurement is that the intrinsic fixture only FEN is at least 15dB lower than the measurement result being evaluated. The spec limit for FEN is -26dB and the corresponding FEN for the fixture assembly alone should be -32dB or lower up

through the signaling 5th harmonic. Test fixture must be verified without mated connectors and connector footprint.

Assuming the -32db FEN fixturing requirements are satisfied, the fixture effects can be ignored and the de-embedded reference planes set to the inputs to the fixture. If the FEN fixturing requirements cannot be satisfied, then their effects need to be de-embedded from the measurements using the procedures outlined in EIA-364-90.

Cables intending to conform to the HBR electrical properties shall be measured against tables outlined in DisplayPort Standard Specification section 4.1.5.3. Cables intending to conform to RBR electrical properties shall be measured against the same profile.

In cases where the dual aggressors are measured individually, the results of the worst two aggressors will be added together to derive the dual aggressor combination.

5.3.5 Pass/Fail Criteria

The observed isolation can be no less than that outlined in the following SDD21 limit masks.

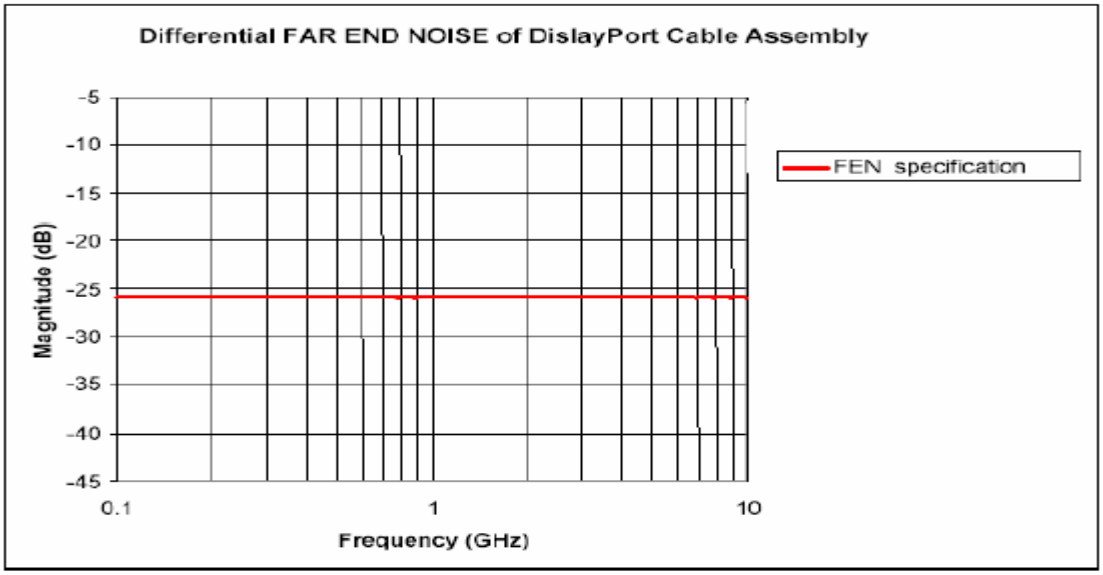

Figure 5-6: Far End Total Noise (peak) for **High** B**it** R**ate** Cable Assembly

Lower Limit Mask. Reference DisplayPort Standard specification section 4.1.5.3 for updates.

Note: Cable Assembly FEN shall reside below limit as shown.

5.4 Bulk Cable and Connector Impedance Measurements (Normative)

5.4.1 Test Objective

The DisplayPort Standard outlines an impedance profile that varies from 10% deviation to 5% deviation on impedance when measuring throughout all significant regions of a cable assembly. This test shall ensure this profile is verified.

(Reference Figures 4-3 and Table 4-1 (Impedance profile values for Cable Assembly) in the VESA DisplayPort Standard)

5.4.2 Interoperability Statement

Bulk Cable

Bulk Cable Impedance defines the nominal impedance and the maximum allowable deviation of the impedance from nominal for a signal of specified rise time within the bulk cable. Typically more tightly controlled than the connector impedance, excessive deviations of the bulk cable impedance from the specified nominal impedance can lead to skew and mode conversion issues in addition to reflections and problems associated with poor return loss performance.

The purpose of the specification limit is to ensure that a specified bulk cable is of suitable performance and quality, and that the tolerances of the bulk cable materials and manufacturing processes are consistent with the signal integrity needs of the application.

Connector

Connector Impedance defines the nominal impedance and the maximum allowable deviation of the impedance from nominal for a signal of specified rise time within the connector region. The connector impedance specification covers the impedance within the regions of the mated connector, wire termination, and wire management regions for which the layout of the signal channel is other than in the bulk cable, or uniform transmission line. Excessive deviations of the connector impedance from the specified nominal impedance can lead to large reflections and problems associated with poor return loss performance.

The purpose of the specification limit is to ensure that the magnitude of any impedance discontinuities encountered by the signal in the connector region of the channel are small enough to allow the input signal to be accurately recovered at the receiver.

5.4.3 Test Conditions

If a family of cables is being tested, any length may be tested for this requirement.

Bulk impedance measurement will observe the impedance vs. time profile of a bulk interconnect region of the cable assembly assuming a 130ps 20/80 transition time.

Cable will be un-rolled and made relatively straight (minimum bend radius of .5m) before making these measurements. Adjacent unused channels shall be terminated into suitable 50 ohm loads.

5.4.4 Measurement Requirements

Special attention to the fixtures is required in performing Impedance measurements. The instrument grade receptacle fixture with no cable present is required be capable of propagating a 50ps (20/80) edge (the edge of the output step) to be considered functional for this test. This test

should be demonstrated on either the 2X calibration trace on the receptacle board, or through a mated plug-receptacle connector pair.

This measurement should be conducted from the non-equalized end of a cable should one exist.

Note: When measuring very long cables skin effect will measured value.

Bulk cable: Special care should be observed to properly address skin loss effects which are not part of this measurement. As such the bulk cable assembly is limited to a 5% impedance deviation centered around 100 Ohms. Skin loss phenomenon results in a slow monotonic increase of observed impedance which is principally a measurement artifact.

The main focus is not the point where the absolute impedance may exceed the 5% tolerance relative to the beginning of the cable assembly, but rather to look for any nominal bumps or dips in the impedance profile which exceed the 5% limit over a 180 ps time interval.

5.4.5 Pass/Fail Criteria

Bulk Cable Portion: The observed impedance should be within the limits of 5% of 100 Ohms through the cable region of the cable assembly. Refer to Table 5-1.

Connector portion: The observed impedance should be within the limits of 10% of 100 Ohms through the connector region of the cable assembly. Both sides of the cable assembly are required to be tested, and shall pass these conditions.

Table 5-1: Impedance and Tolerances

Segment	Differential Impedance Value	Maximum Tolerance	Comment
Fixture	100 Ω	± 10%	Fixture shall have trace lengths of no more than 3 cm (1.18”)
Connector	100 Ω		
Cable Management	100 Ω		Transition from ±10% to ±5% shall have a slope of 5Ω/80ps
Cable	100 Ω	± 5%	

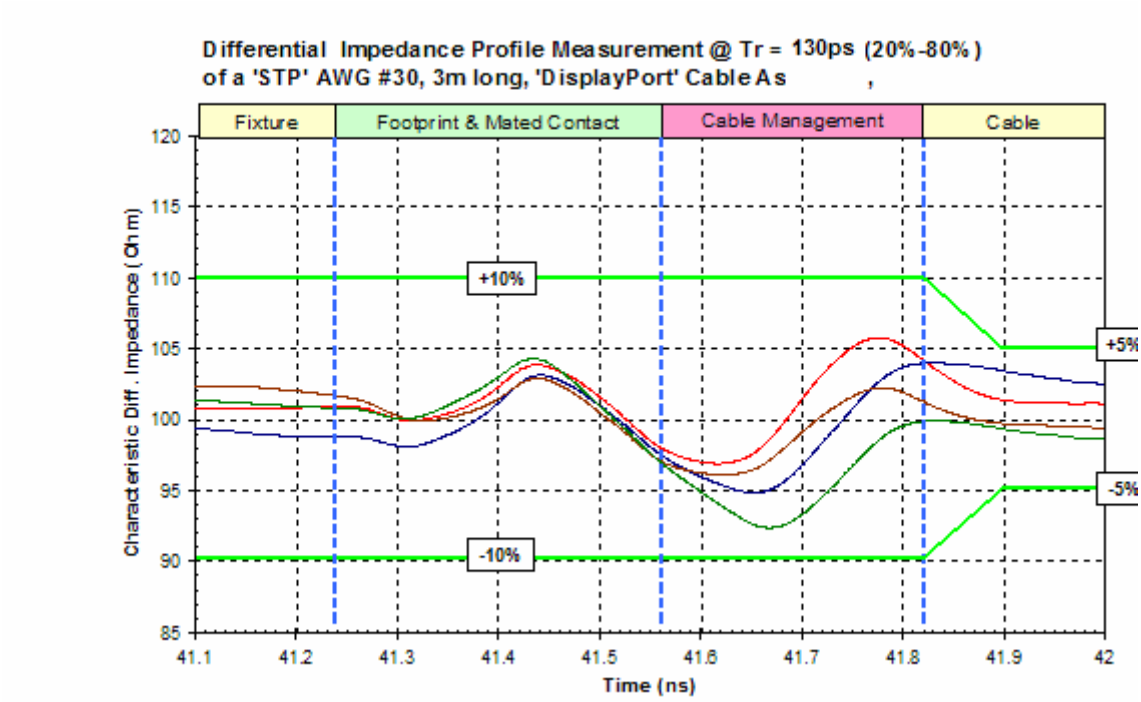

Figure 5-7: Impedance Profile Measurement Impedance Limits & Connector Profile Example

Reference VESA DisplayPort Standard Section 4.1.3.

Note: Bulk Cable Impedance shall reside within the 5% limits.

5.5 Insertion Loss (IL/SDD21) Measurements (Normative)

5.5.1 Test Objective

The DisplayPort Standard outlines two distinct differential Insertion Loss (SDD21) profiles. One of the high bit rate cable assembly and one corresponding profile for the lower bit rate cable assembly. This test outlines the pass fail criteria around these two tests.

(Reference Figures 4-4 and 4-10 (Mixed Mode Differential Insertion Loss for High bit rate Cable Assembly SDD21 profiles) in the VESA DisplayPort Standard).

5.5.2 Interoperability Statement

Insertion loss defines the sink to source loss through the channel. The magnitude of the insertion loss especially at low frequencies has a significant effect on the eye height of the received signal. In general a signal channel acts as a low pass filter and the change of insertion loss with frequency has important consequences for the rise time degradation and hence the maximum supportable bandwidth of the channel. Channels for which the insertion loss characteristics show increased high frequency loss can suffer significant ISI and Jitter due to the spreading of the signal edges caused by rise time degradation.

The purpose of the specification limit is to ensure that the necessary eye height and width are maintained to allow the input signal to be accurately recovered at the receiver.

5.5.3 Test Conditions

If a family of cables is being tested, shortest and longest lengths are tested for this requirement.

SDD21 shall be evaluated and compared to the corresponding limits mask, from 100MHz to 7 GHz.

Cable will be un-rolled and made relatively straight (minimum bend radius of .5m) before making these measurements.

5.5.4 Measurement Requirements

Prior to the measurement, proper calibration shall be performed to either remove (de-embed) the effects of the test fixture through any null recognized calibration method or include the test fixture effects by implementing SOLT calibration method using standard calibration kit (supplied with the test instrument) to set up the measurement reference plane at the coaxial connectors mounted on the test fixture.

5.5.5 Pass/Fail Criteria

The observed insertion loss shall be no less than that outlined in the following SDD21 limit masks.

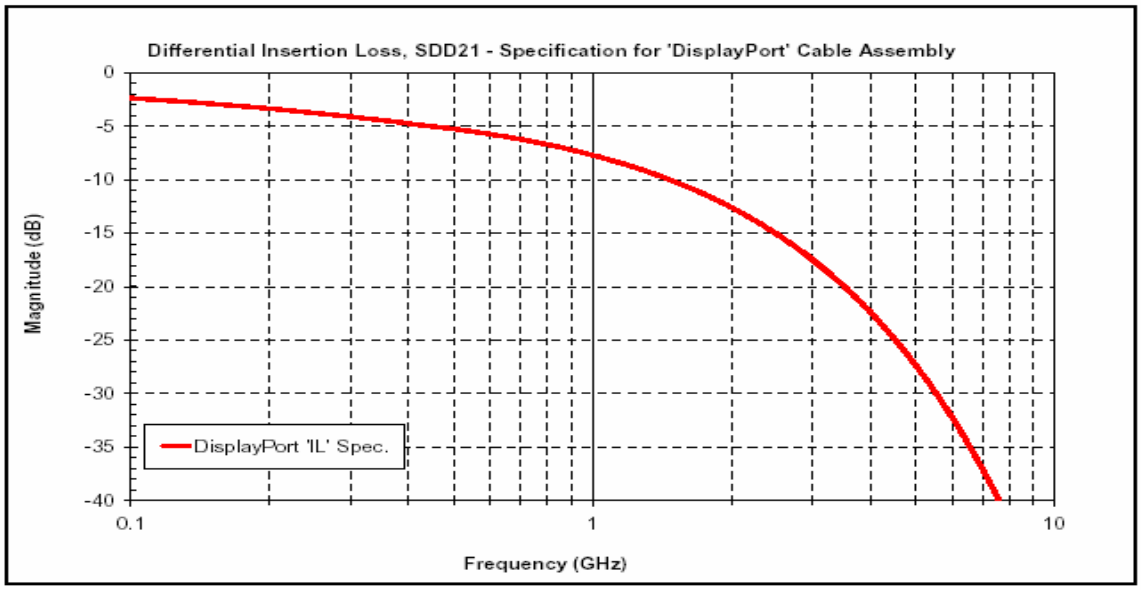

Figure 5-8: Mixed Mode Differential Insertion Loss for High Bit Rate Cable Assembly

Lower Limit Mask. Reference VESA DisplayPort Standard Section 4.1.5.1.2 (Return Loss Upper Limit for High Bit Rate Cable Assemblies).

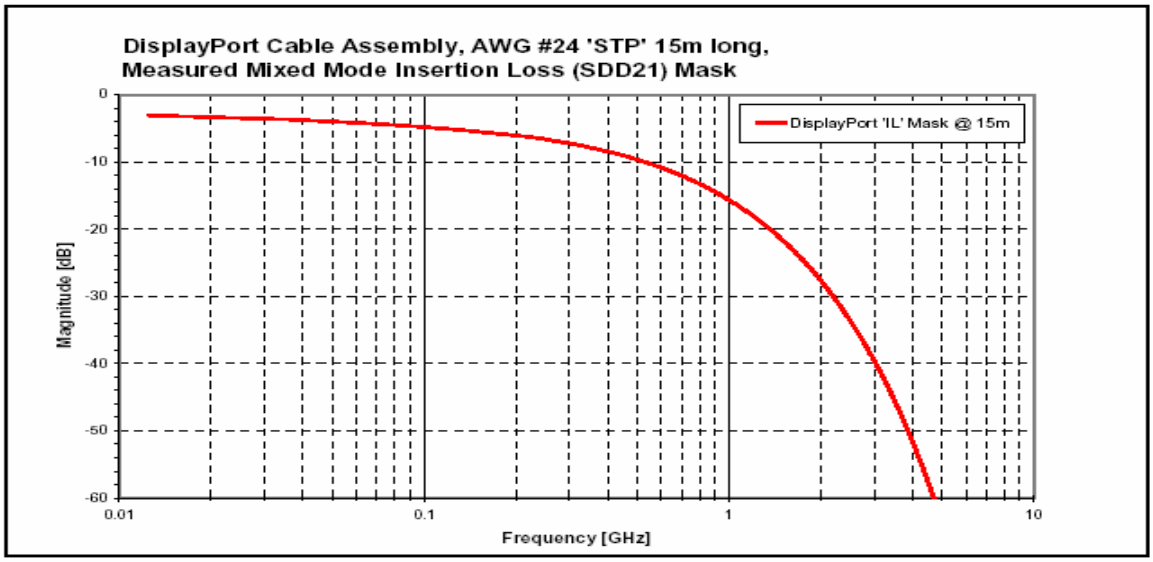

Figure 5-9: Mixed Mode Differential Insertion Loss for Low Bit Rate Cable Assembly

Lower Limit Mask. Reference DisplayPort Standard 4.1.6.1.2 (Return Loss Upper Limit for High Bit Rate Cable Assemblies) for updates.

Note: Cable Assembly SDD21 shall reside above the profile listed above.

5.6 Near End Noise (NEN) Measurements (Normative for AUX Channel, Informative for Data Channel)

5.6.1 Test Objective

The DisplayPort Standard outlines two distinct Near End Noise (NEN) profiles. One of the high bit rate cable assembly and one corresponding profile for the lower bit rate cable assembly. This test outlines the pass fail criteria around these two tests.

(Reference Figures 4-6 and 4-12 (Near End Total Noise (peak) HBR/RBR Cable Assembly NEN profiles) in the VESA DisplayPort Standard)

5.6.2 Interoperability Statement

Near End Differential Noise defines the magnitude of the inductive and capacitive coupled noise from a driven "aggressor" channel (or channels), on to a quiet "victim" channel. Near end noise specifically refers to the differential noise level measured on the victim channel at the source side of the channel, relative to a differential signal or signals originating at the source side of an aggressor channel (or channels). Near end noise can significantly distort the received signal leading to jitter and ISI issues for the received signal.

The purpose of the specification limit is to ensure that the level of differential noise seen by a signal on the "victim" channel due to near end noise coupling is below a maximum allowable level necessary to ensure that an accurate representation of the input signal can be recovered by the receiver.

5.6.3 Test Conditions

NEN is a near end isolation SDD21 (near end to near end) measurement and shall be evaluated and compared to the corresponding limits mask, from 100MHz to 7 GHz.

The principal focus of the Differential NEN measurement on both ends of the link.

On Source side it is the differential NEN induced on AUX Channel from Main Link as illustrated on figure 5-10

On Sink side, it is the differential NEN induced on Main Link from AUX Channel as illustrated in figure 5-11.

Cable will be un-rolled and made relatively straight (minimum bend radius of .5m) before making these measurements. If a family of cables is being tested, any cable length may be tested for this requirement. *Note: the rationale is that Near End Noise is not cable length dependent.*

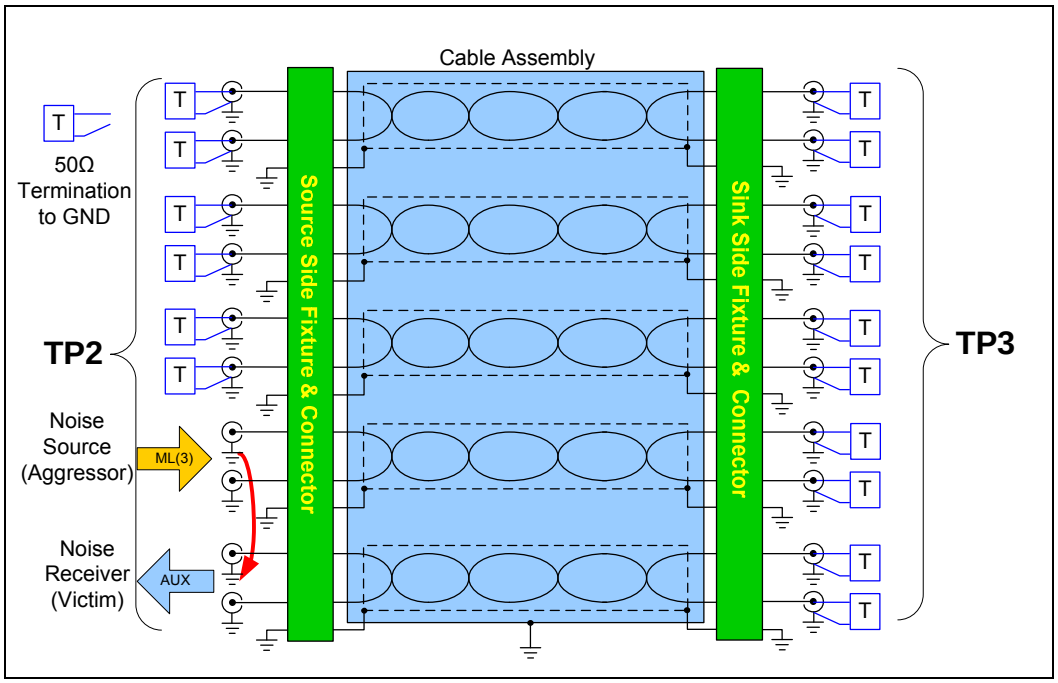

Figure 5-10: Near End Noise (peak) measurement configuration at the Source side

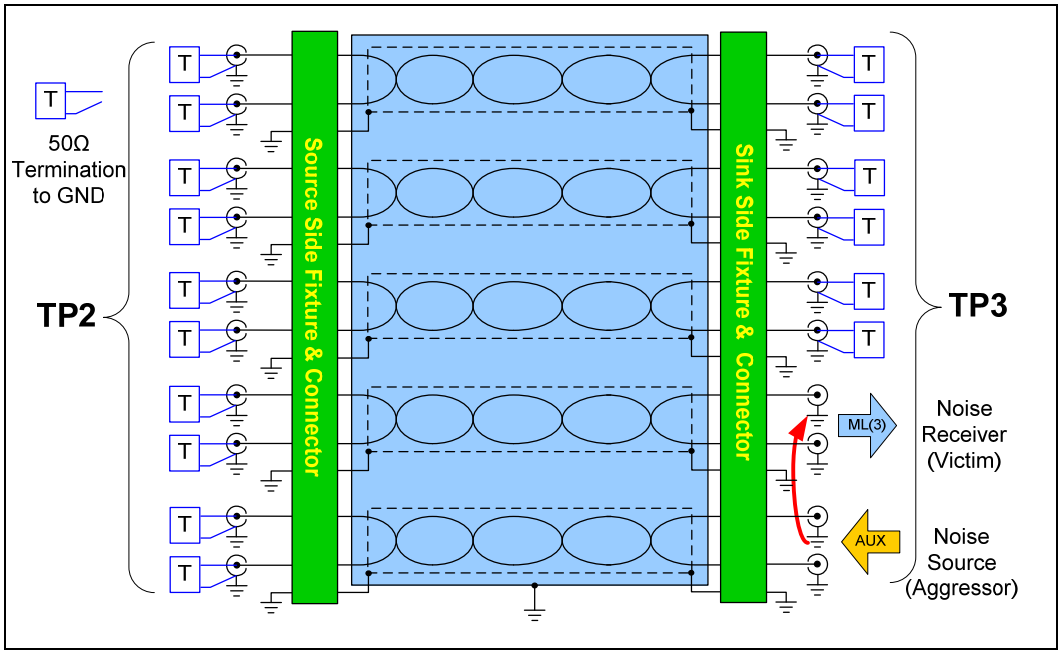

Figure 5-11: Near End Noise (peak) measurement configuration at the Sink side

5.6.4 Measurement Requirements

Special attention to the fixtures is required in performing NEN measurements. The figure of merit to determine if a fixture is suitable to perform a NEN is if the intrinsic fixture only NEN is at least 15dB lower than the measurement result being evaluated. The spec limit for NEN is -26dB and the corresponding NEN for the fixture assembly alone should be -32dB or lower up through the signaling 5th harmonic. The Test Fixture must be verified without mated connectors and connector footprint.

All the NEN measurements are performed differentially.

Assuming the -32db NEN fixturing requirements are satisfied, the fixture effects can be ignored and the de-embed reference planes set to the inputs to the fixture. If the NEN fixturing requirements cannot be satisfied, then their effects need to be de-embedded from the measurements using the procedures outlined in EIA-364-90.

Cables intending to conform to the HBR electrical properties shall be measured against tables outlined in DisplayPort Standard Specification section 4.1.5.2. Cables intending to conform to RBR electrical properties shall be measured against tables outlined in the VESA DisplayPort Standard Section 4.1.6.2.

5.6.5 Pass/Fail Criteria

The observed insertion loss can be no less than that outlined in the following SDD21 limit masks.

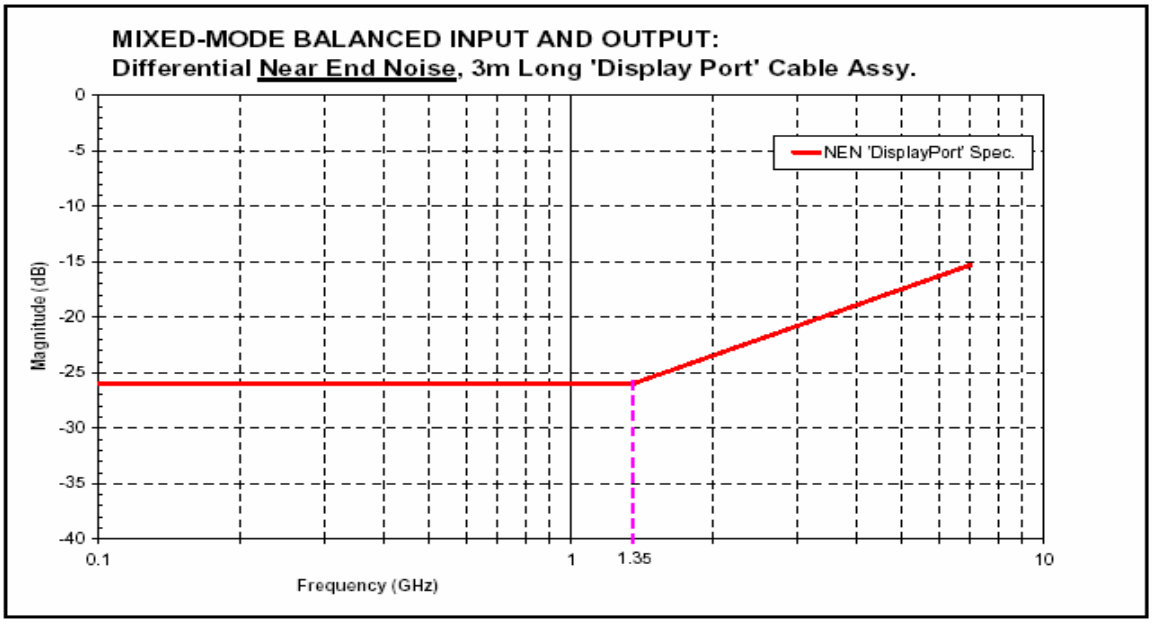

Figure 5-12: Near End Total Noise (peak) for High Bit Rate Cable Assembly

Lower Limit Mask. Reference VESA DisplayPort Standard 4.1.5.2.

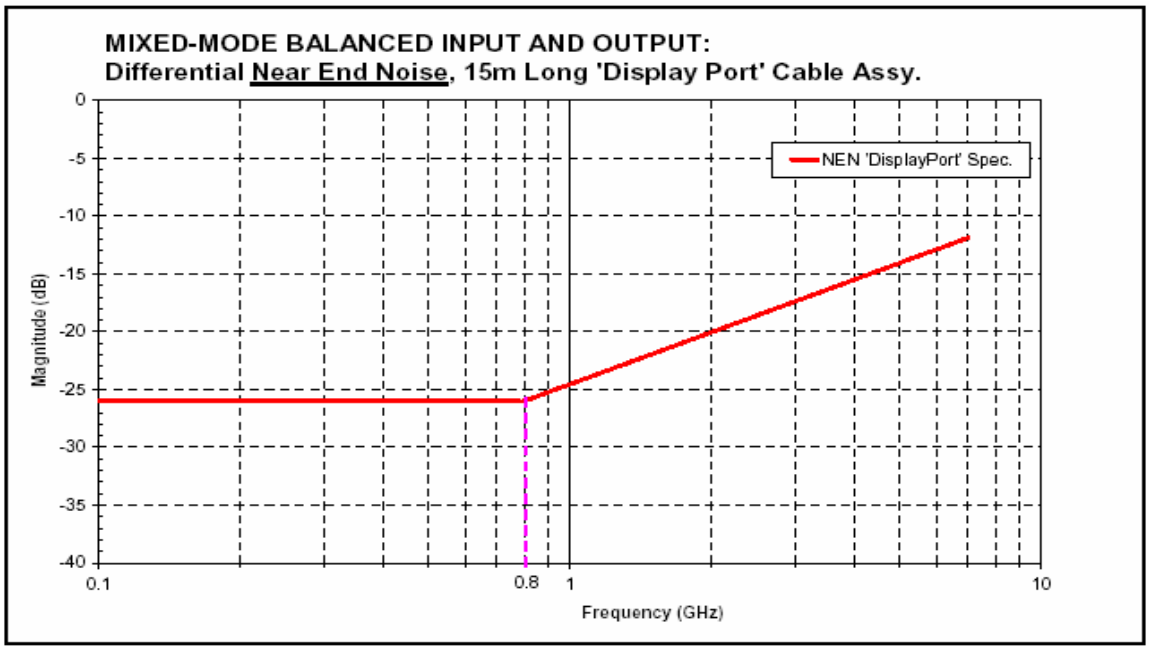

Figure 5-13: Near End Total Noise (peak) for Reduced Bit Rate Cable Assembly

Lower Limit Mask. Reference VESA DisplayPort Specification 4.1.6.2 .

Note: Cable Assembly NEN shall reside below the profile listed above.

5.7 Return Loss (RL/SDD11) Measurements (Normative)

5.7.1 Test Objective

The VESA DisplayPort Standard outlines two distinct differential Return Loss (SDD11) profiles. One of the high bit rate cable assembly and one corresponding profile for the reduced bit rate cable assembly. This test outlines the pass fail criteria around these two tests.

Reference Figures 4-5 and 4-11 (Mixed Mode Differential Return Loss for HBR/RBR Cable Assembly SDD11 profiles) in the VESA DisplayPort Standard

5.7.2 Interoperability Statement

Return Loss Defines the ratio of the incident and reflected power for a channel. Reflections originate at impedance discontinuities within the channel, and reflected signals can strongly affect the rising edge of the signal, negatively impacting the signal rise time, intra-pair skew, and Jitter. Excessive reflected signal can give rise to resonant loss which causes increased frequency selective insertion loss.

The purpose of the specification limit is to ensure that the eye height is not closed due to reflection generated loss and that the eye width is not compromised reflection generated jitter in order to allow the input signal to be accurately recovered at the receiver.

5.7.3 Test Conditions

SDD11 shall be evaluated and compared to the corresponding limits mask, from 100MHz to 7 GHz.

All cable lengths shall be tested.

Cable will be un-rolled and made relatively straight (minimum bend radius of .5m) before making these measurements.

5.7.4 Measurement Requirements

Prior to the measurement, proper calibration shall be performed to either remove (de-embed) the effects of the test fixture through any null recognized calibration method or include the test fixture effects by implementing SOLT calibration method using standard calibration kit (supplied with the test instrument) to set up the measurement reference plane at the coaxial connectors mounted on the test fixture.

5.7.5 Pass/Fail Criteria

The observed return loss shall be no more than that outlined in the following SDD11 limit masks.

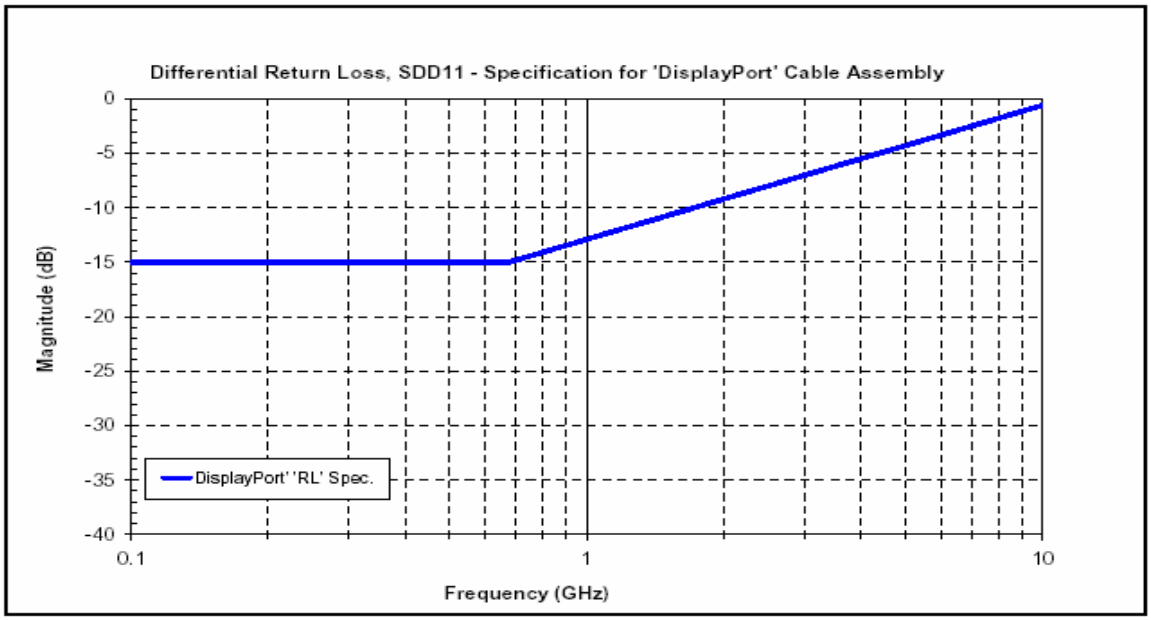

Figure 5-14: Mixed Mode Differential Return Loss for High Bit Rate Cable Assembly

Lower Limit Mask. Reference VESA DisplayPort Standard Section 4.1.5.1.2 (Return Loss Upper Limit for High Bit Rate Cable Assemblies).

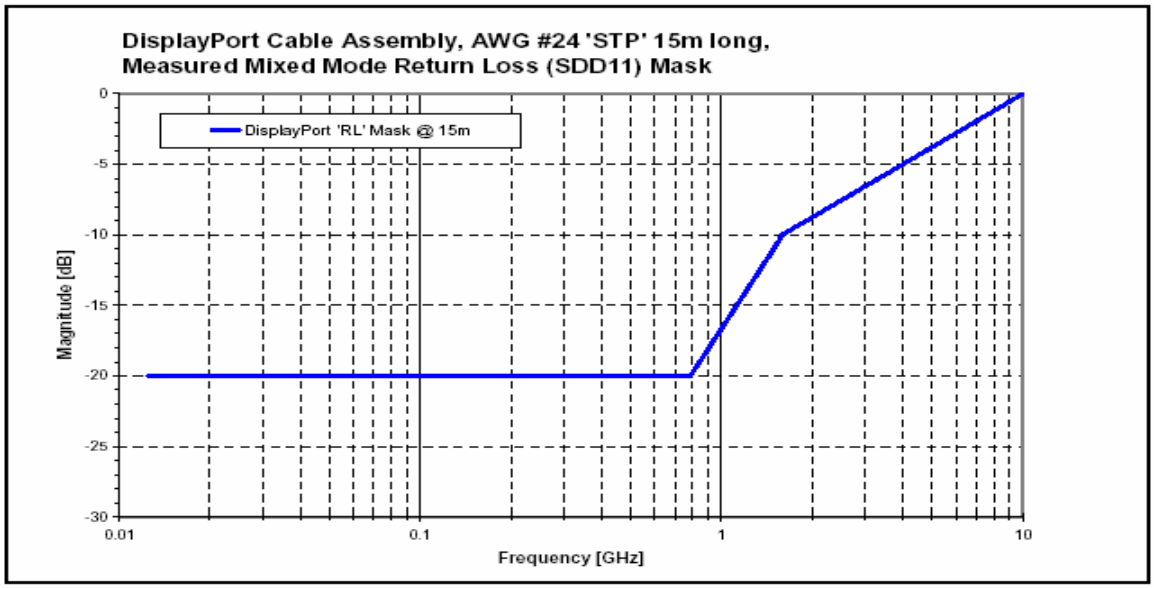

Figure 5-15: Mixed Mode Differential Return Loss for Low Bit Rate Cable Assembly

Lower Limit Mask. Reference VESA DisplayPort Standard 4.1.6.1.2 (Return Loss Upper Limit for High Bit Rate Cable Assemblies).

Note: Cable Assembly SDD11 shall reside below the profile listed above.

6 Hybrid Devices Compliance Tests

6.1 Hybrid Devices Definition

A Hybrid Device is any device that is not an originating Source or destination Sink, but is responsible for transporting data between one or more Sources to one or more Sinks by means other than that provided for by the Physical Layer as defined in Section 3 and Mechanical, Cable-Connector Assembly Specifications as defined in Section 4-1 of the DisplayPort Standard. A Hybrid Device may consist of a pair of sub-devices that use alternative wired or wire-free means including optical or radio technology to connect sub-devices. These sub-devices shall transport the link layer as defined in Section 2. The interface to these sub-devices shall meet the interface requirements of Source and Sink respectively.

This section specifies the PHY layer characteristics of a Hybrid Device and the tests that shall be performed to verify that Hybrid Devices will operate as designed in a DisplayPort environment. Hybrid Devices with short tethered cables to input or output connectors shall be treated as mate-direct devices and shall pass these compliance tests. Other "dongle" devices are NOT covered in this section.

6.2 Physical Description

All Hybrid Devices shall be designed to mate-directly to the DisplayPort connector on a Source Device. This requires a DisplayPort "Plug" gender connector at the input to the Hybrid Device. Hybrid Devices as of this release shall not be required to support Source Devices with tethered cables as defined in section 7.1.

The output connector gender of a Hybrid Device is determined by the "Type" of Sink Device connection.

Two types of Sink Device connections are supported by the Hybrid Device Outputs:

The first Type is "D" for "detachable" cable function.

In this case a Sink Device has a panel mounted "Socket" intended to mate with a detachable cable.

Type "D" Hybrid Devices shall mate-directly to the "Socket" on the Sink Device using a "Plug" gender connector attached to the Hybrid Device.

Type "D" devices shall be designed to mate-directly to a "Socket" connector mounted on the Source, and mate-directly to a "Socket" connector mounted on the Sink. Type "D" devices function as a substitute for a cable.

Notes:

1. The term "mate-directly" shall mean that no additional separable cable is allowed in the signal path.
2. No support for pre-emphases is provided at either end of a Type "D" Hybrid Device.

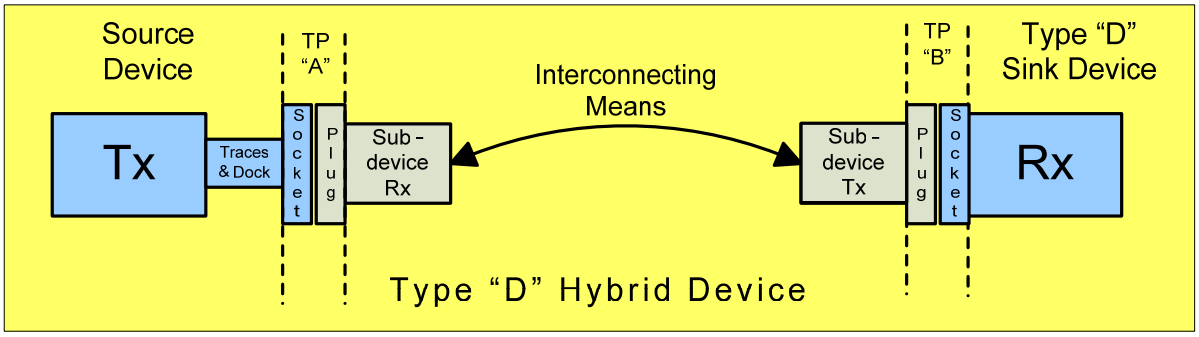

Figure 6-1: Type "D" Hybrid Device Configuration

The second Type is "T" for "tethered" cable.

In this case a Sink Device uses a tethered cable with "Plug" or a connected detachable cable; that is intended to mate with the "Socket" mounted on a Source.

Type "T" devices shall mate-directly with the "Plug" on a tethered cable attached to the Sink Device or connect via detachable cable, mating with the "Socket" gender connector mounted on the Hybrid Device.

Type "T" devices shall be designed to mate-directly to a "Socket" connector mounted on the Source, and mate-directly to a Sink via tethered cable attached to the Sink or mate remotely to a Sink via detachable cable, in both latter cases via a "Socket" connector mounted on the Hybrid Device.

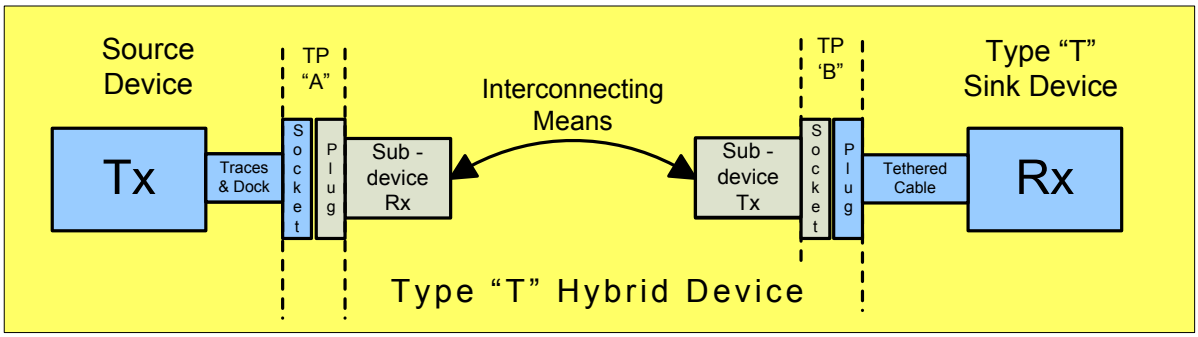

Figure 6-2 : Type "T" Hybrid Device Configuration

Type "D" and "T" devices have physically different connectors at their output. Type "D" devices shall have a "Plug" connector to mate-directly to a "Socket" connector on a Sink. Type "T" devices shall have a "Socket" connector, that mimics the "Socket" connector of a Source Device, the intended connection point of a detachable or tethered cable.

Table 6.1 – Connector Requirements for Hybrid Devices

Hybrid Device Type	Input Connector Type	Output Connector Type
D	Plug	Plug
T	Plug	Socket

6.2.1 Hybrid Device Compliance Tests and Setup

Hybrid Devices shall be designed to transport data from an originating Source Device to a terminating Sink Device. To assure operability with all DisplayPort functions, the input to a Hybrid Device shall behave as a Sink that is connected using a zero length of cable. The Type "D" output shall provide signal quality greater than or equal to those present at the Sink end of a maximum length of cable as defined for TP 3'. The Type "T" output shall behave as a Source intended to drive a maximum length of cable as defined for TP 2'.

The Hybrid Device Compliance Tests are designed to ensure that three test results are achieved.

1. When connected to a Sink, the Hybrid Device shall be capable of correctly receiving a data stream originating from a worst-case Source Device under the installation conditions mandated by the manufacturer of the link.
2. When connected to a Source, the data stream measured at the output of the Hybrid Device shall meet the requirements necessary to ensure error-free reception by a worst-case Sink Device.
3. All AUX functions shall be supported by the Hybrid Device

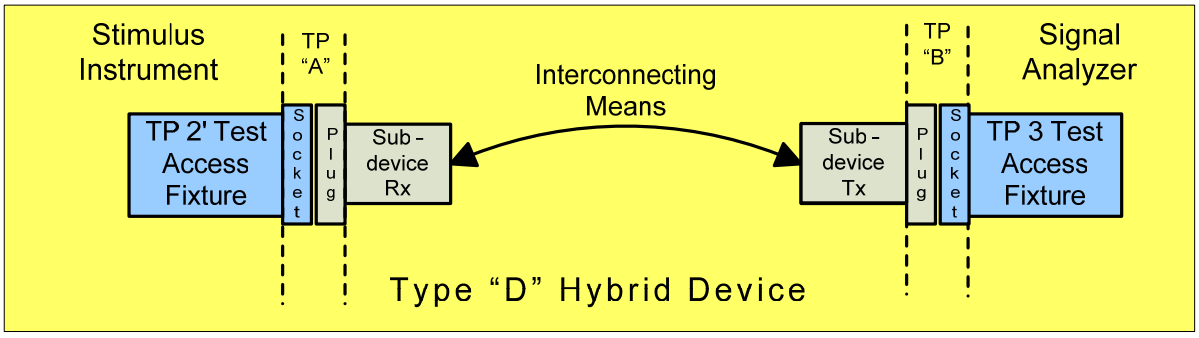

Figure 6-3: Type "D" Hybrid Device Test Configuration

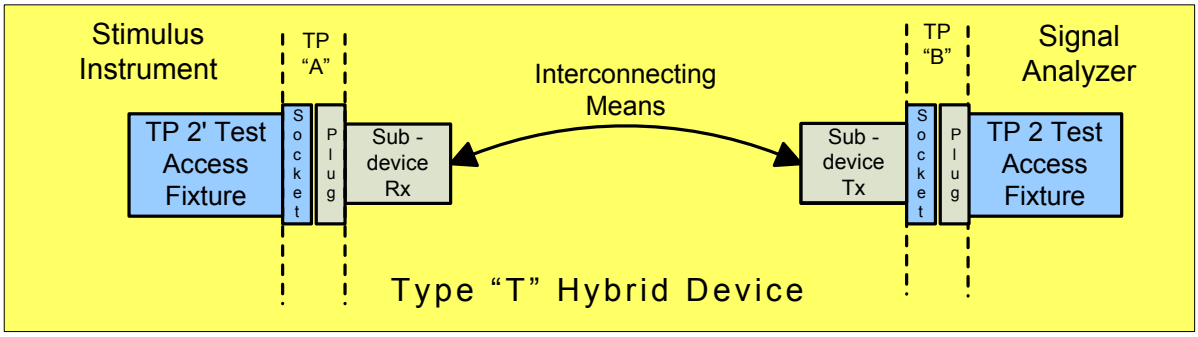

Figure 6-4: Type "T" Hybrid Device Test Configuration

6.2.2 Test Menu

Proper support of AUX channel functions is covered in the Link Layer Compliance Document. In order to ensure verification of objectives 1 and 2, Hybrid Device shall be tested using the test methods described in previous sections of this document, as required. The following tests are required to verify such performance. The appropriate section number in this document is shown in parentheses. These tests for Hybrid devices carry the same informative/normative properties as the referenced tests.

1. Eye Diagram (3.1)
2. Non Pre-Emphasis Level Verification Testing (3.2)
3. Pre-Emphasis Level Verification Testing (3.3)
4. Inter-pair Skew (3.4)
5. Intra-pair Skew (3.5)
6. Differential Transition Time (3.6)
7. Single-Ended Transition Time (3.7)
8. Overshoot and Undershoot (3.8)
9. Frequency Accuracy (3.9)
10. AC Common Mode Noise (3.10)
11. ISI Jitter Measurements (3.11)
12. Total Jitter (TJ) Measurements (3.12)
13. Receiver BER Measurements (4.1)
14. Far End Noise Tests (5.3)
15. Near End Noise Tests (5.7)
16. AUX channel Tests (Link Layer compliance test Specification)
17. Hybrid Device Input Tests
18. Hybrid Device Output Tests
19. Hybrid Device Cable Tests

Each test requirement is discussed separately in the following sections.

6.3 Eye Diagram

The eye diagram test procedures described in Section 3.1 shall be applied to the output of the Hybrid Device with the input stimulus provided by a Source Device. All requirements of Section 3.1 shall be met by the Hybrid Device.

6.4 Level Verification

Type “D” Devices

Level verification for Type “D” devices at the output of the device shall meet the requirements of the Non Pre-Emphasis Level Verification Tests as described in Section 3.2 while the device is connected to a Source Device.

Type “T” Devices

Level verification for Type “T” devices at the output of the device shall meet the requirements of the Pre-Emphasis Level Verification Tests as described in Section 3.3 while the device is connected to a Source Device.

6.5 Inter-pair Skew

Inter-pair skew measurements shall be performed at the output of a Hybrid Device with the device connected to a Source Device according to the procedures described in Section 3.4 of this document. All requirements shall be met.

6.6 Intra-pair Skew

Intra-pair skew measurements shall be performed at the output of a Hybrid Device with the device connected to a Source Device according to the procedures described in Section 3.5 of this document. All requirements shall be met.

6.7 Differential Transition Time

Differential Transition Time measurements shall be performed at the output of a Hybrid Device with the device connected to a Source Device according to the procedures described in Section 3.6 of this document. All requirements shall be met.

6.8 Single-Ended Transition Time

Single-Ended Transition Time measurements shall be performed at the output of a Hybrid Device with the device connected to a Source Device according to the procedures described in Section 3.7 of this document. All requirements shall be met.

6.9 Overshoot and Undershoot Tests

The Hybrid Device shall be connected to a Source Device. Overshoot and undershoot measurements shall be made at the output of the Hybrid Device according to the procedures described in Section 3.8 of this document. This test is informative.

6.10 Frequency Accuracy

The Hybrid Device shall be connected to a Source Device. Frequency accuracy measurements shall be made at the output of the Hybrid Device according to the procedures described in Section 3.9 of this document. All requirements shall be met.

6.11 AC Common Mode Noise

The Hybrid Device shall be connected to a Source Device. AC common mode noise tests shall be made at the output of the Hybrid Device according to the procedures described in Section 3.10 of this document. All requirements shall be met.

6.12 Non-ISI Jitter Test

The Hybrid Device shall be connected to a Source Device. Deterministic jitter measurements shall be made at the output of the Hybrid Device according to the procedures described in Section 3.11 of this document. All requirements shall be met.

6.13 Total Jitter Test

The Hybrid Device shall be connected to a Source Device. ISI jitter measurements shall be made at the output of the Hybrid Device according to the procedures described in Section 3.12 of this document. All requirements shall be met.

6.14 BER Tests

Hybrid Devices are intended to be mate-directly to a Source Device. For the purpose of testing the input of the Hybrid Device, a worst case Source Stimulate test signal shall be applied at TP "A" via a TP 2' Test Access Fixture. This test signal may be supplied either from a Source Device or from a suitable BER test set. The receiver tests described in Section 4.1 shall be completed satisfactorily. All requirements shall be met.

6.15 Far End Noise

The Hybrid Device shall be connected to a Source Device. Far end noise measurements shall be made at the output of the Hybrid Device according to the procedures described in Section 5.3 of this document. All requirements shall be met.

6.16 Near End Noise

The Hybrid Device shall be connected to a Source Device. Near end noise measurements shall be made at the output of the Hybrid Device according to the procedures described in Section 5.7 of this document. All requirements shall be met.

6.17 AUX channel Tests

The Hybrid Device shall be connected to AUX channel testers at TP "A" and TP "B". The AUX channel shall be verified using HPD and EDID read tests as specified in the Link Layer specification.

6.18 Hybrid Device Input Tests

Type "D" and "T" tests shall comprise the use of a TP 2' Stimulus instrument at TP "A" set as appropriate for signal stimulus, and a TP 3 Test Access Fixture at TP "B" that shall verify the test.

Note: Pre-Emphasis is NOT supported at the TP "A" interface.

6.19 Hybrid Device Output Tests

The Hybrid Device is tested as one of two types.

Type "D" Hybrid Device

The Type "D" test shall comprise the use of a TP 2' Stimulus instrument at TP "A" and a TP 3 Test Access Fixture at TP "B" and the measured signals shall adhere to eye mask specifications for a TP3.

Note: Pre-Emphasis is NOT supported at either interface!

Type "T" Hybrid Device

The Type “T” test shall comprise the use of a TP 2’ Stimulus instrument at TP “A” and a TP 2 Test Access Fixture at TP “B” and the measured signals shall adhere to eye mask specifications for the TP2.

Note: Pre-Emphasis is supported at interface TP “B” ONLY!

6.20 Hybrid Device Cable Tests

The Hybrid Device shall be connected to a Stimulus instrument at TP “A” and a signal analyzer at TP “B”.

7 Tethered Devices

This section defines the electrical test requirements for complex devices comprised of a cable permanently attached to either a source or a sink. Such devices are conceived to address specific market requirements and have narrow application.

Note that in the following sections, the references to TP2, TP2', TP3 and TP3' refer to the same definitions found in section 2.2.

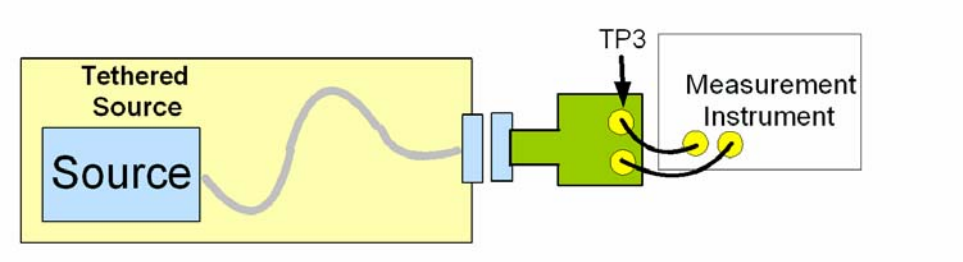

Figure 7-1: Tethered Source Connection to Measurement Equipment

7.1 Source with Tethered Cable

Many system vendors will consider permanent attachment of a cable to the source.

It is clear that considerations must be made on the measurement test point identified as the Test Point.

There are two specific cases:

1. Tethered source connector is Plug:

   The test at the test point shall be made using the TP 3 Test Access Fixture and shall adhere to eye mask and AUX specifications for TP3.

2. Tethered source connector is Receptacle:

The tests at the Test Point shall be made using the TP 2 Test Access Fixture and shall adhere to eye mask and AUX specifications for TP2.

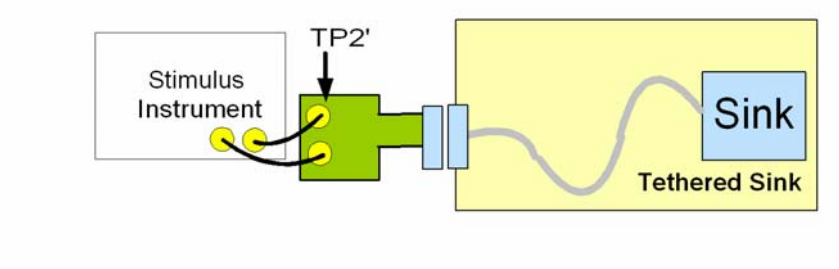

Figure 7-2: Tethered Sink and Test Equipment Connection

7.2 Sink with Tethered Cable

Vendors of Sinks will also consider having captive cables.

There are two specific cases:

1. Tethered Sink connector is Plug:

   The tests at the Test Point shall be made using the TP 2' Test Access Fixture and shall adhere to stressed eye and AUX generation equivalent to TP2'.

2. Tethered Sink connector is Receptacle:

The tests at the Test Point shall be made using the TP 3' Test Access Fixture and shall adhere to stressed eye and AUX generation equivalent to TP3'.